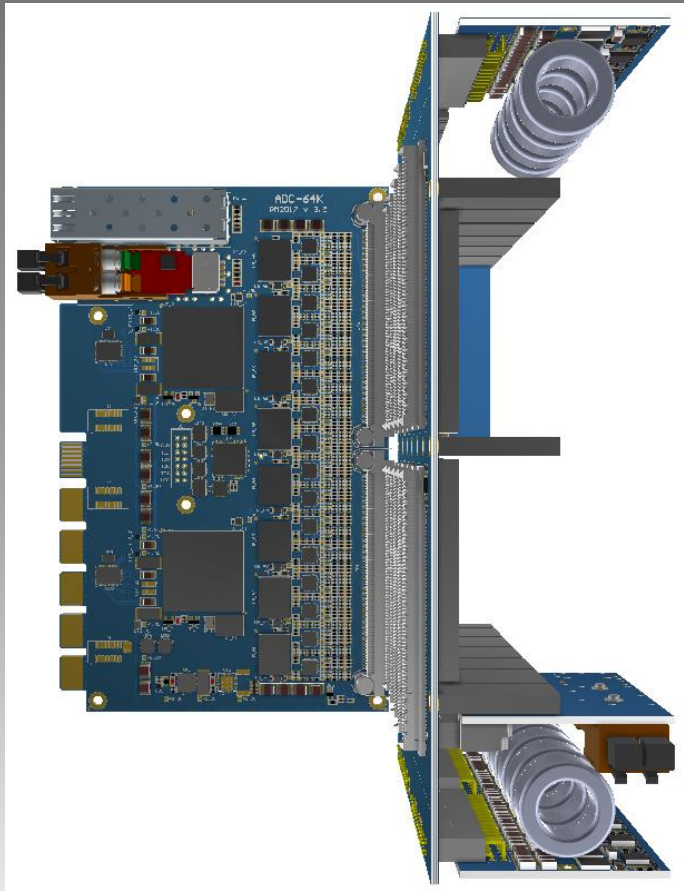
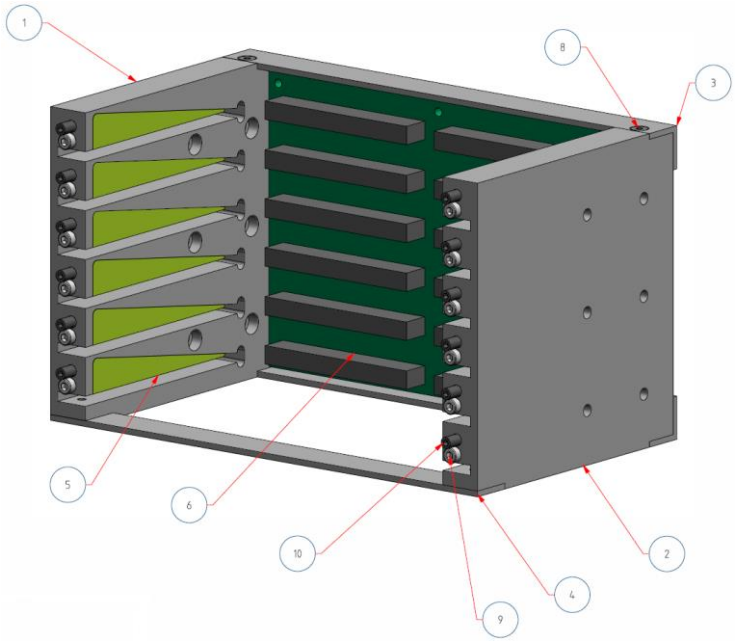
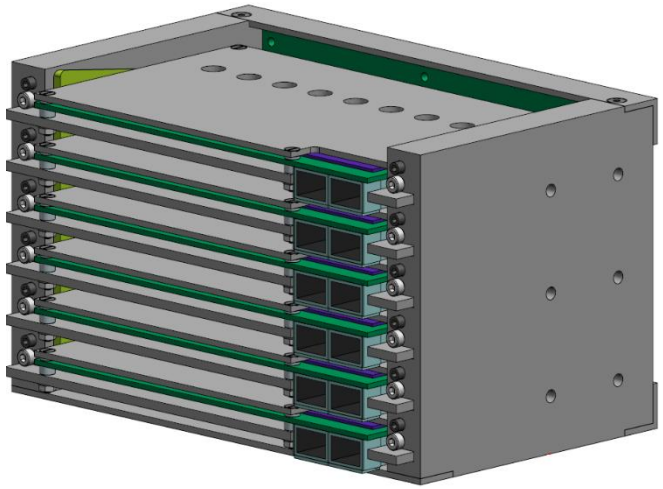
ADC Crate
Rear Compartment

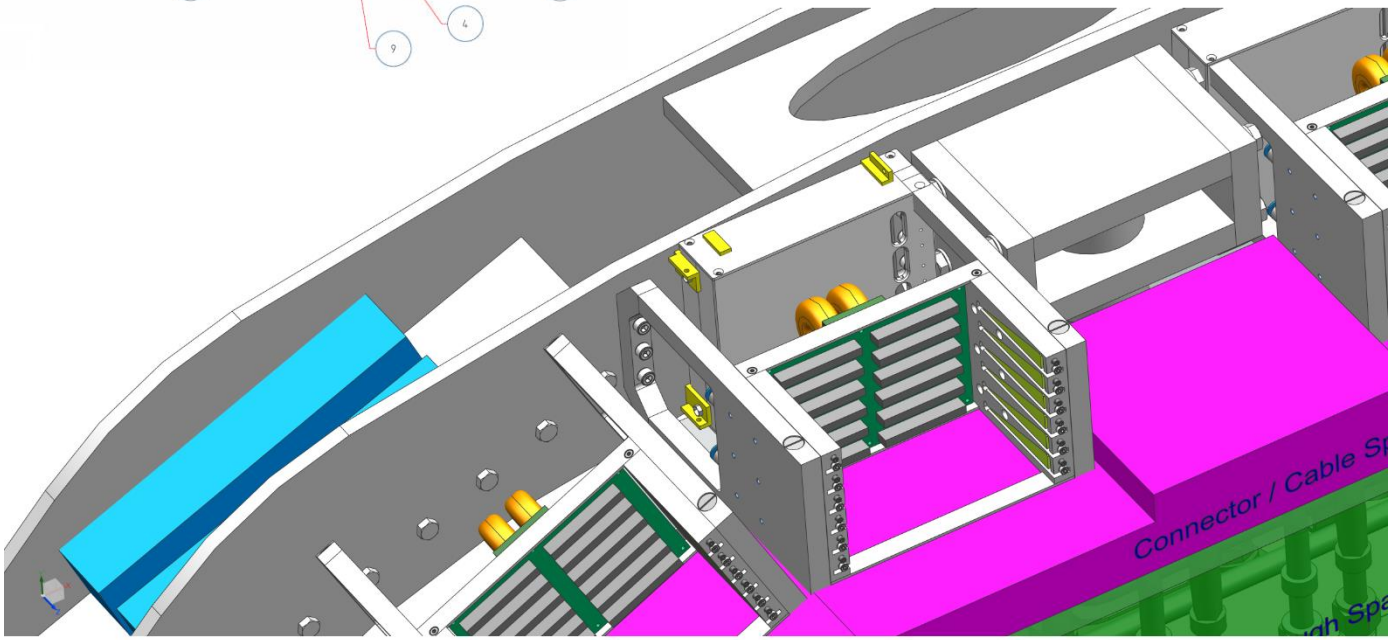


ADC for EMC-Endcap

- Encapsulation and Cooling







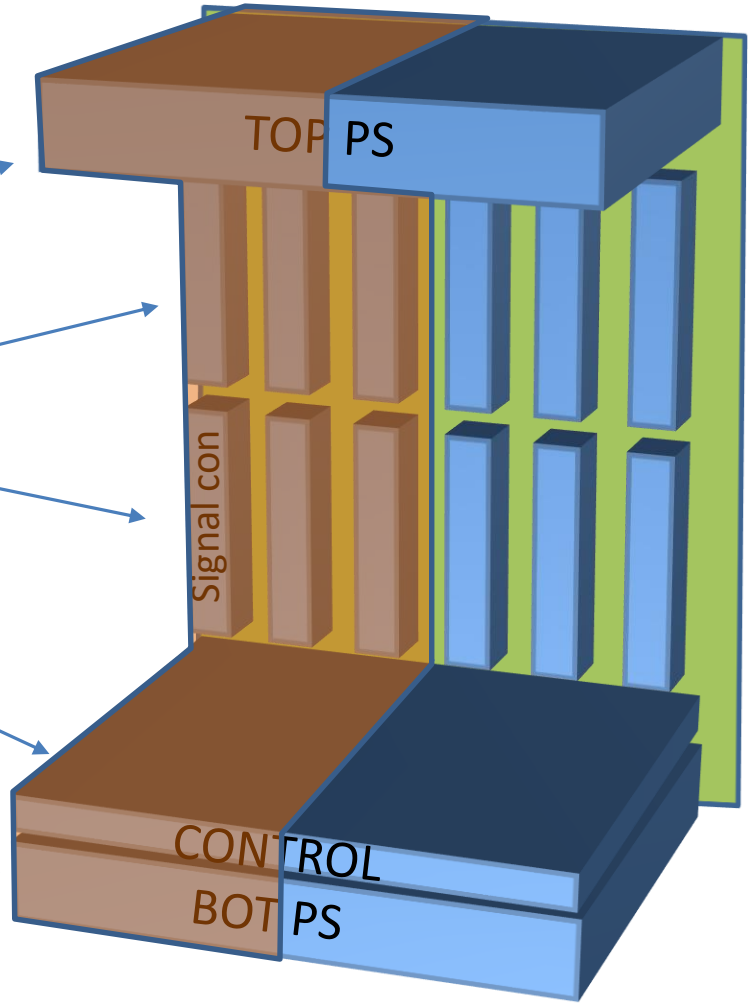
Courtesy KVI

- Crate backplane preparation

Backward crate compartment

- **TOP Power Supply (Digital 1.0V, 1.5V, 2.5V, 3.3V)**
- **Signal connectors**
- **Crate Control**
- **Bottom Power Supply (Analog 2.5V)**

Tripple slot module division



ADC for EMC-Endcap

- Crate backplane preparation

TRIPLE SLOT MODULE

TX/RX - GTX Triple module loop (HF buffered)

Can be used for re-routing of faulty main transceivers or for multiplexing of the readout

I²C AUX – provides differential I2C control for the detector ASICS (requested by Barrel).

Can be used for indicating FPGA configuration status (DONE) to the control system

I²C PWR – For monitoring of the ADC voltages and currents

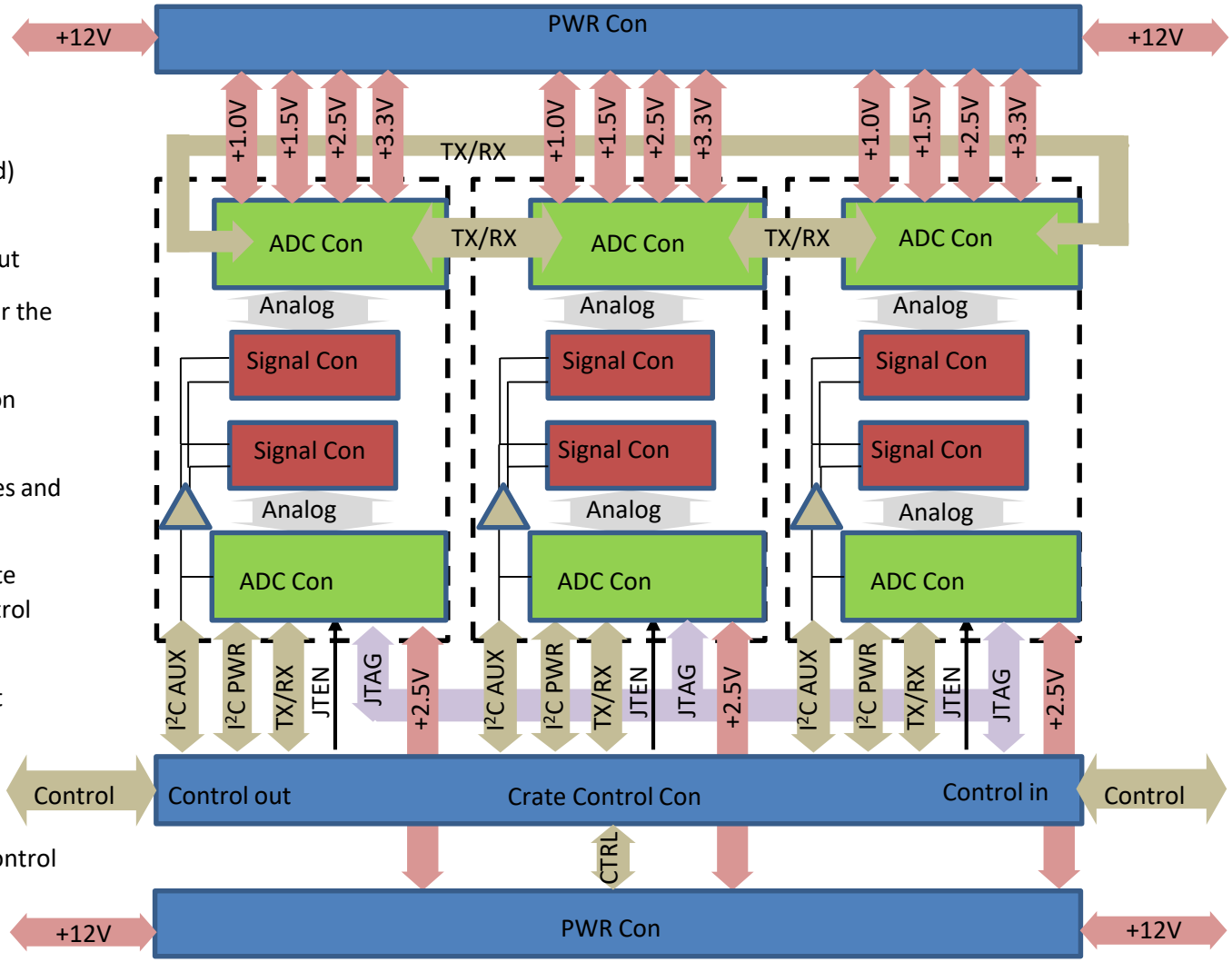
TX/RX – can be freely used inside of the Crate Control board. Either looped or fed to a control FPGA

JTEN – JTAG enable for operation on the slot

JTAG – Common lines (buffered)

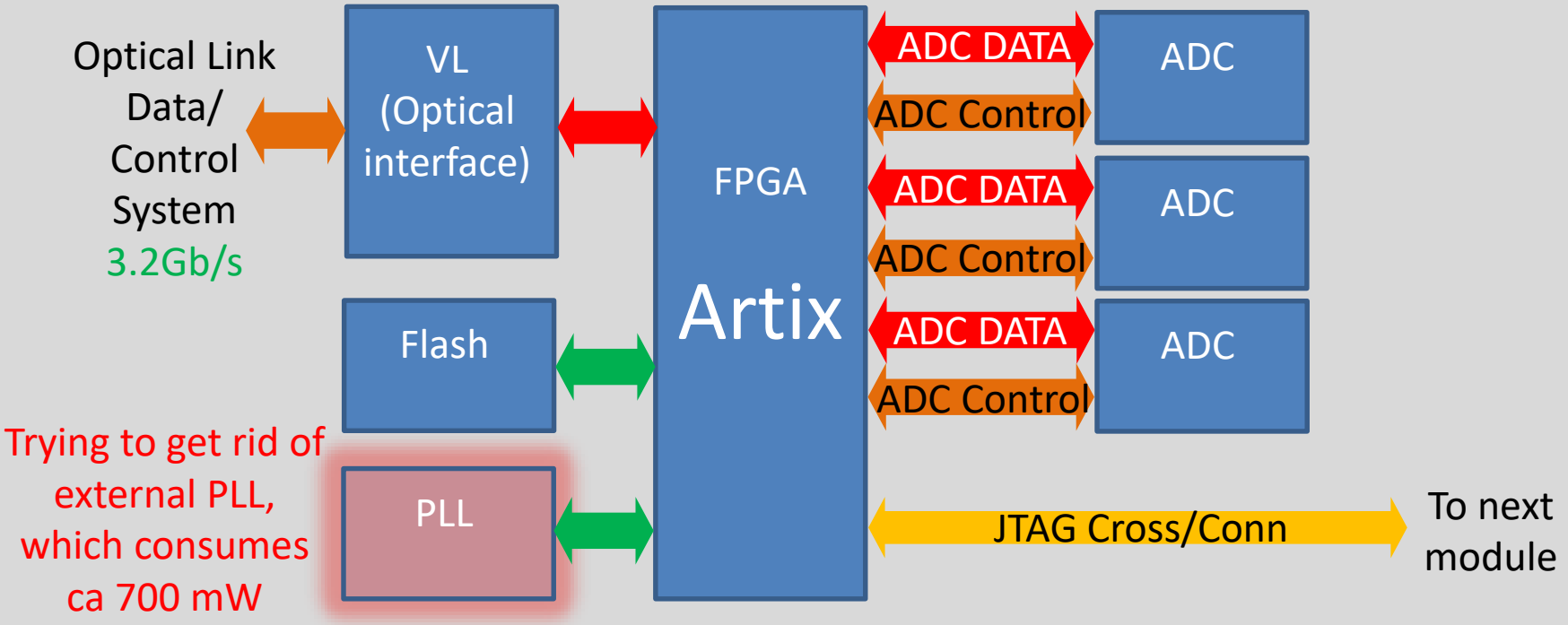
CTRL – PS control

Control – A daisy-chain interface for crate control (optical interface out?)



Crate Control

1. Direct JTAG configuration of individual ADCs
2. Reaction to SEU
3. Health control of ADCs (voltages, currents, temperatures)
4. Crate PS control



Crate Control

Application Note: 7 Series FPGAs and Zynq-7000 AP SoCs

XILINX
ALL PROGRAMMABLE

XAPP589 (v2.3) April 29, 2015

All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000)

Authors: David Taylor, Matt Klein, and Vincent Vendramini

Summary

This application note delivers a system that is designed to replace external voltage-controlled crystal oscillator (VCXO) circuits by utilizing functionality within each serial gigabit transceiver.

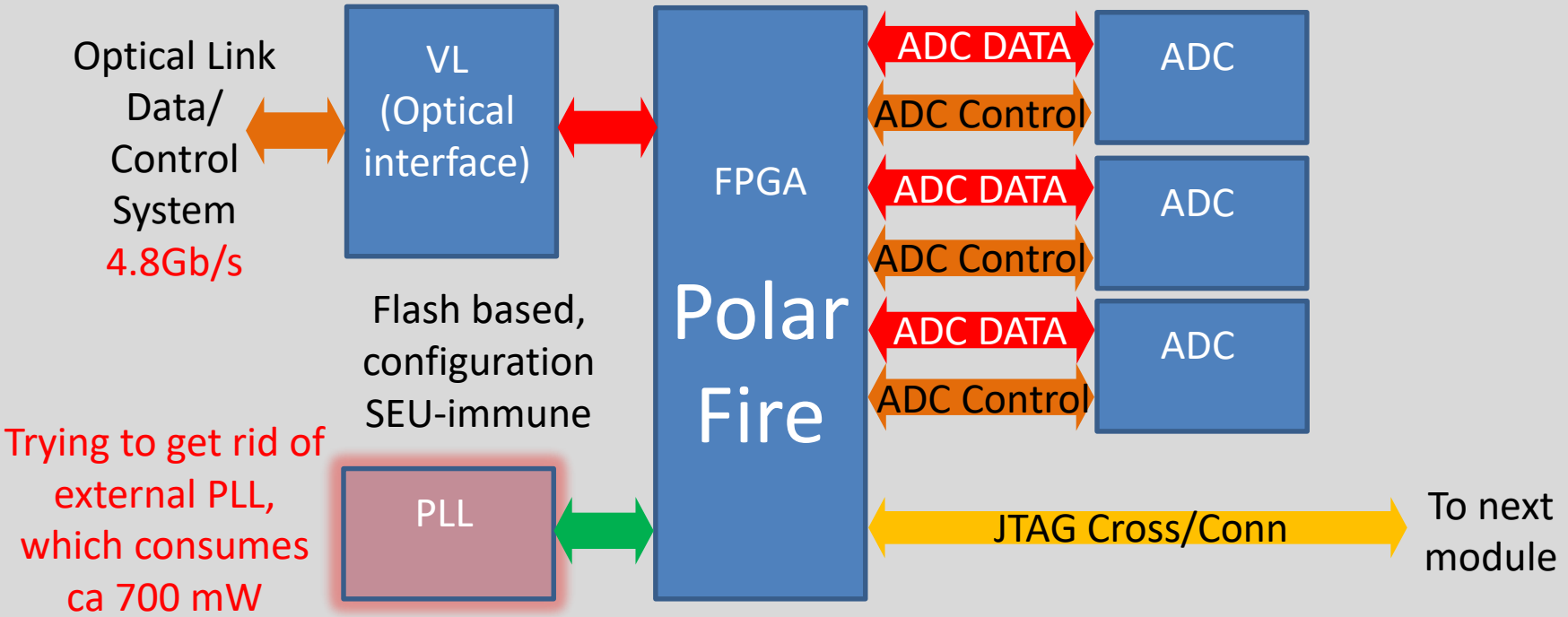
Note: In this application note, *transceiver* refers to these types of transceivers:

Device Family	Transceiver Type
Artix®-7 FPGA	GTP transceiver
Kintex®-7 FPGA	GTX transceiver
Virtex®-7 FPGA	GTX and GTH transceivers
Zynq®-7000 All Programmable SoC	GTP and GTX transceiver

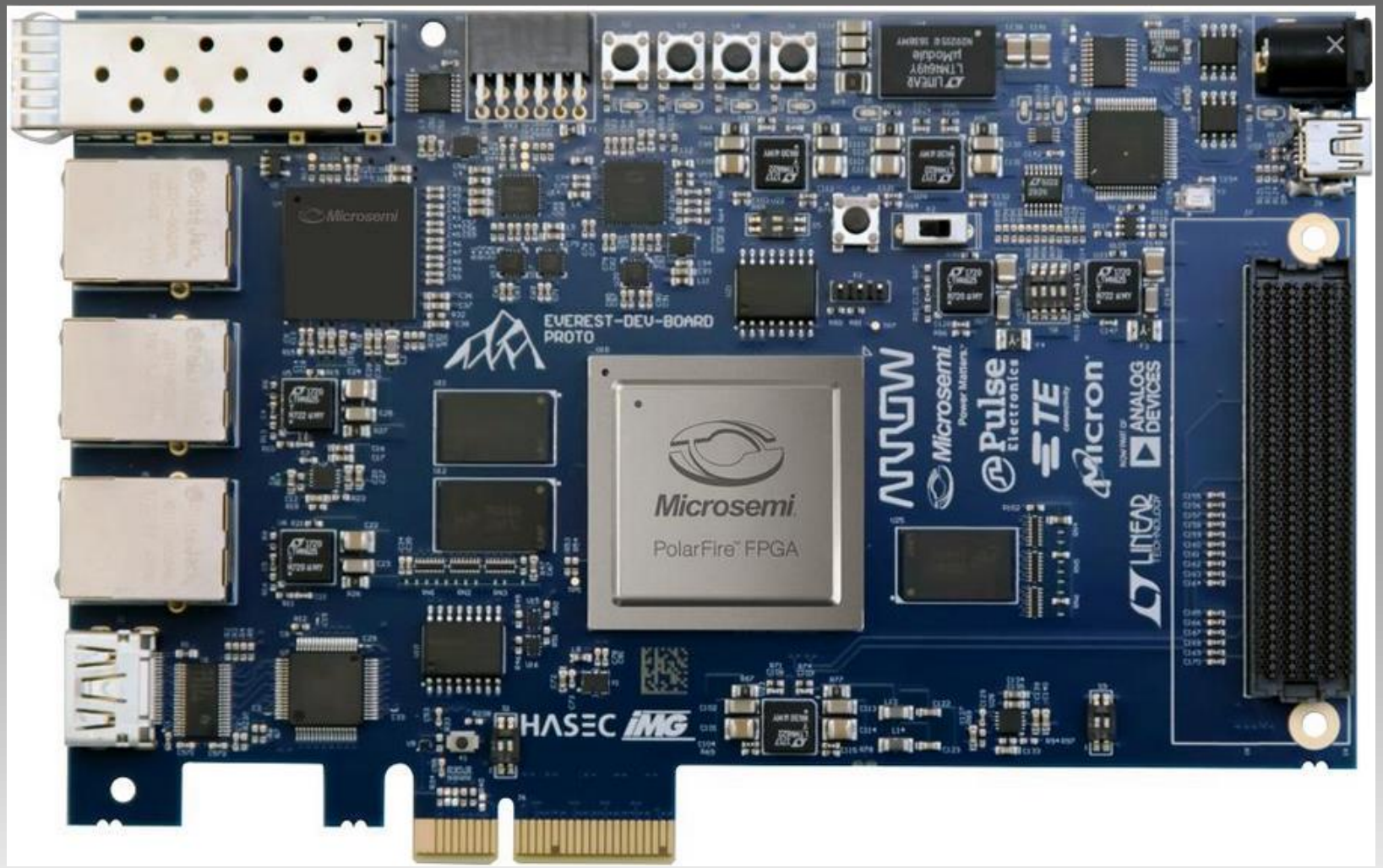
A common design requirement is to frequency or phase lock a transceiver output to an input source (known as loop, recovered, or slave timing). Traditionally, an external clock cleaning

Crate Control

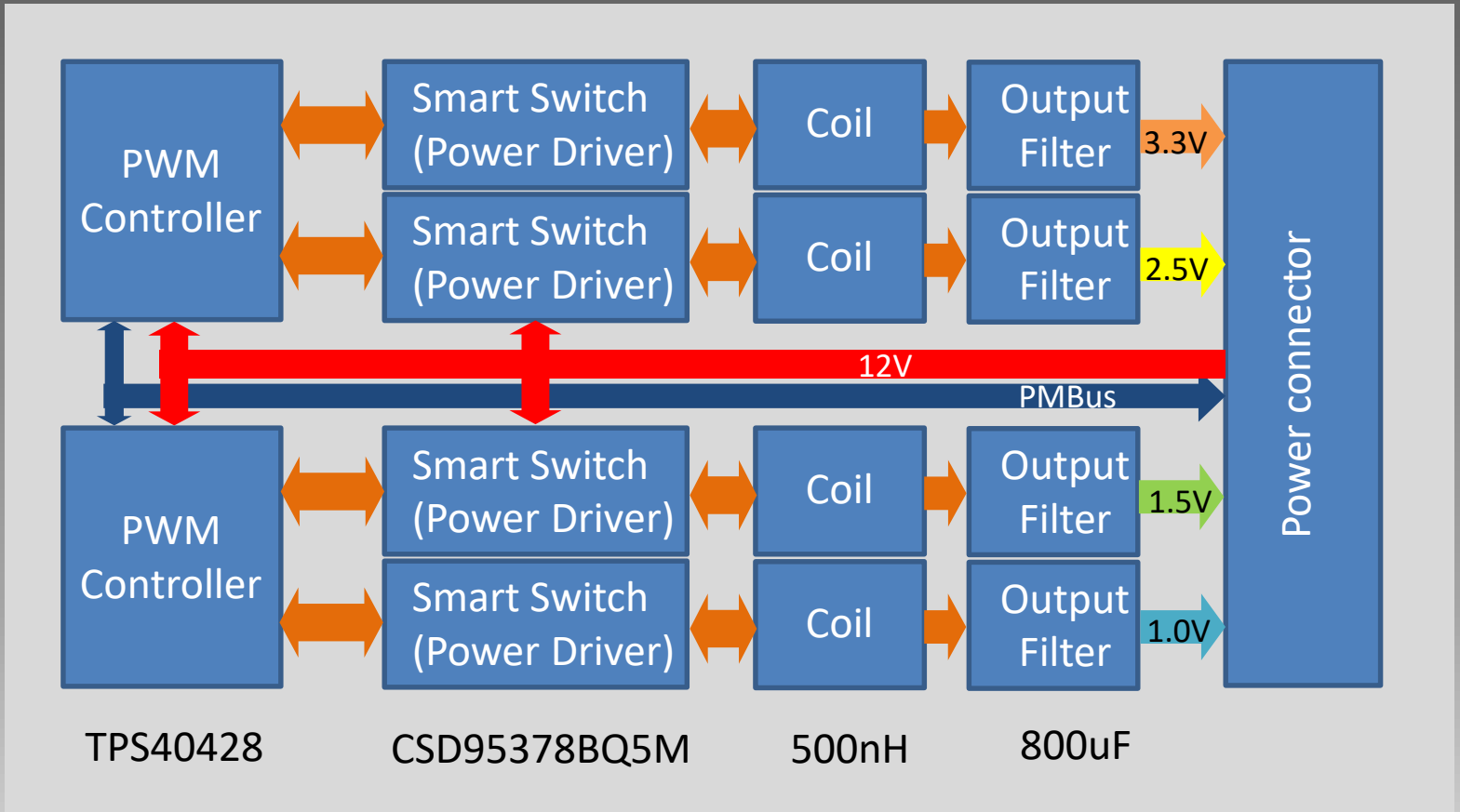
1. Direct JTAG configuration of individual ADCs
2. Reaction to SEU
3. Health control of ADCs (voltages, currents, temperatures)
4. Crate PS control



Crate Control

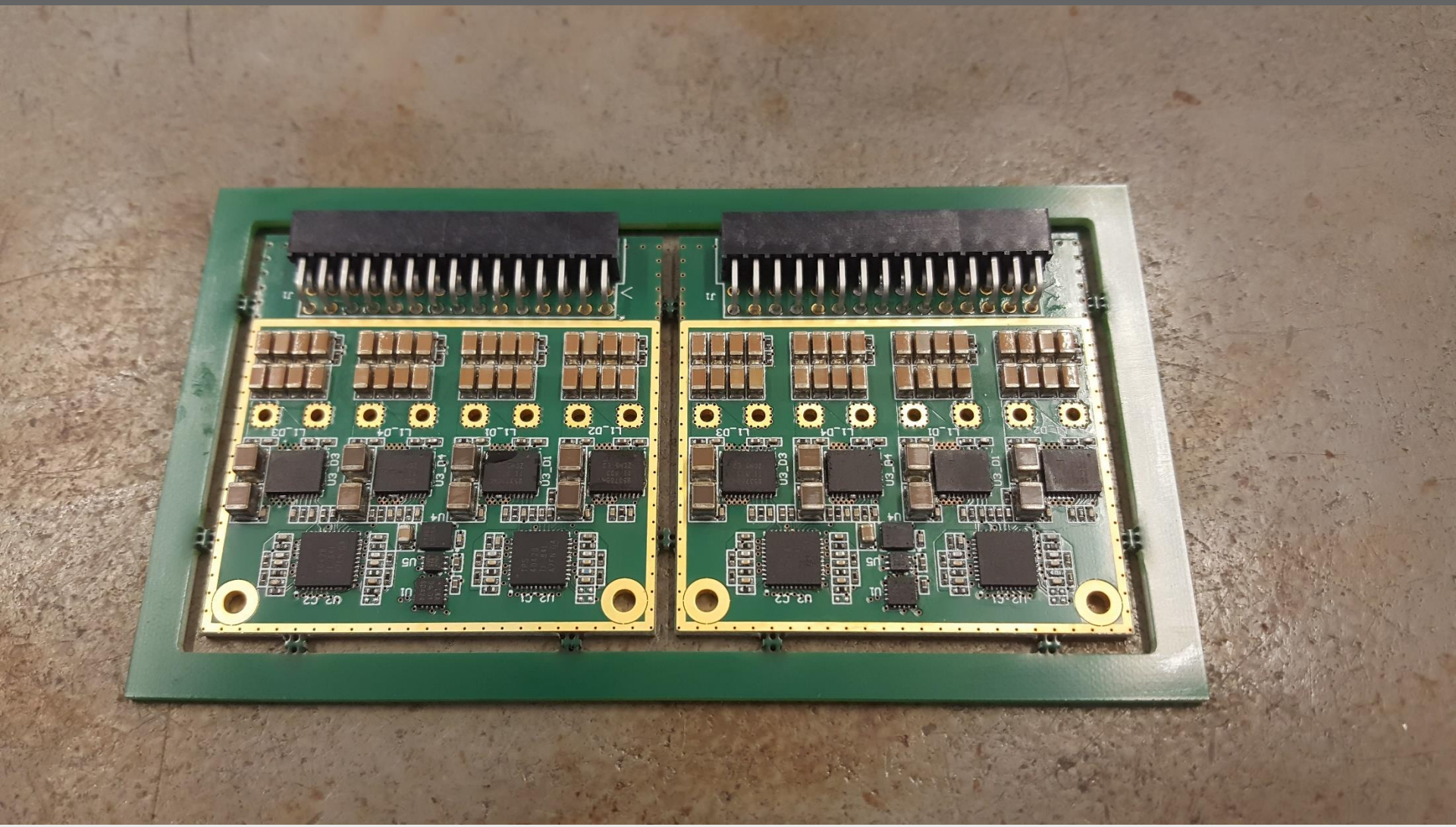


Power Supply

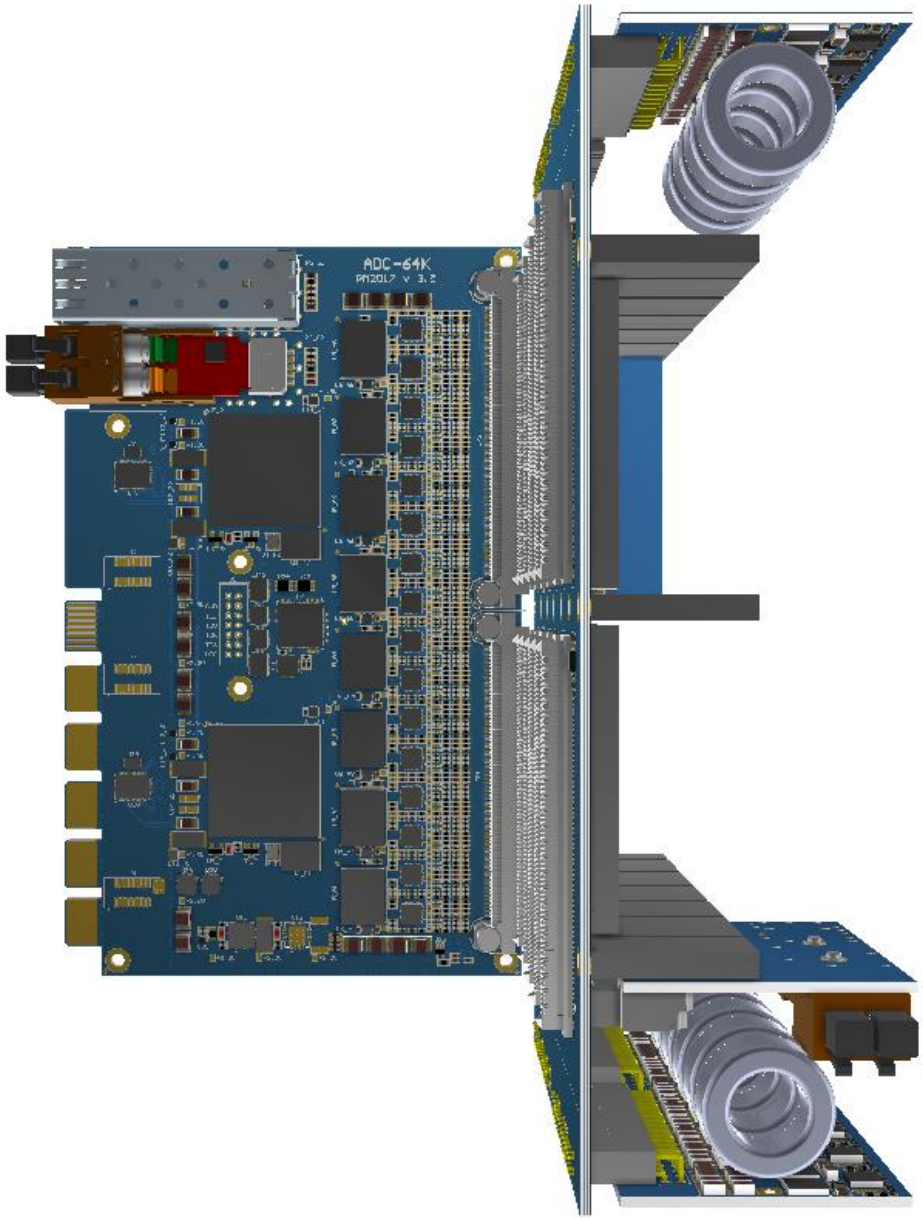


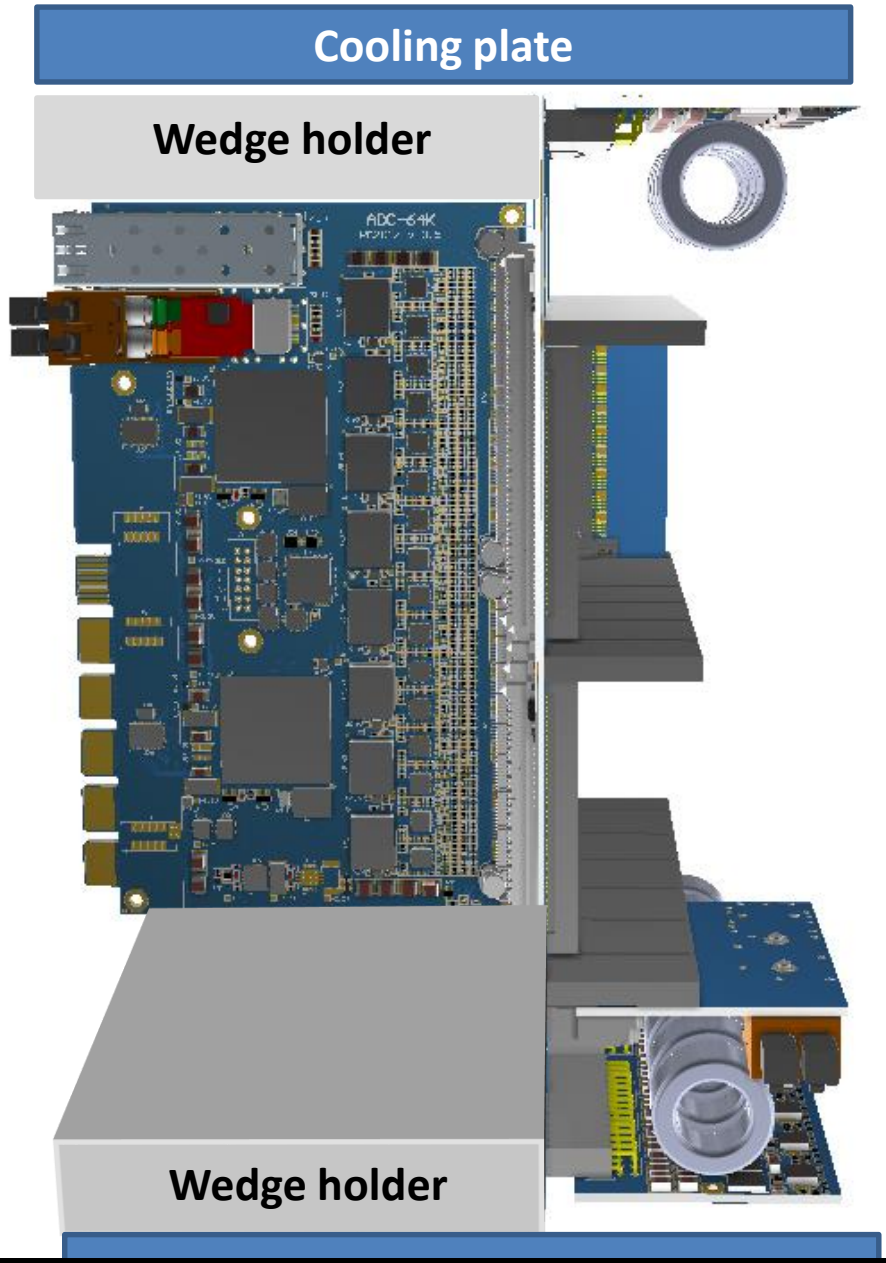
Voltages coarse programmed by resistors.
Fine adjustable by Control System

Power Supply

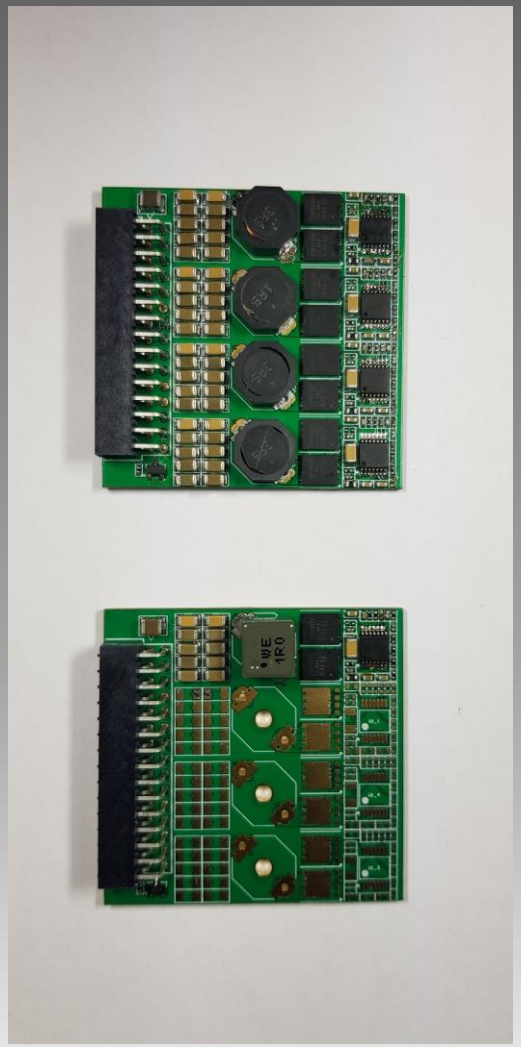


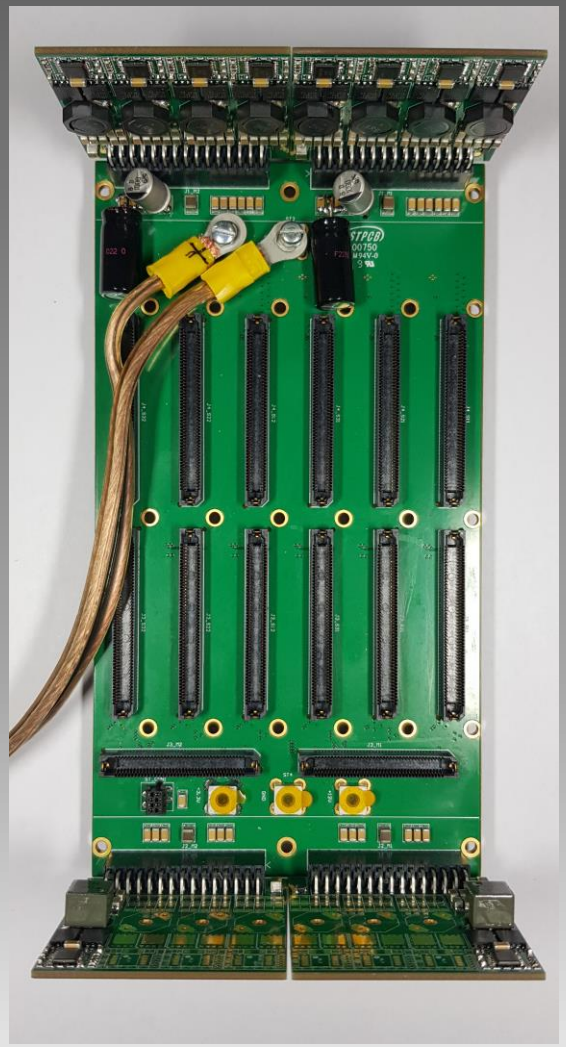
ADC for EMC-Endcap

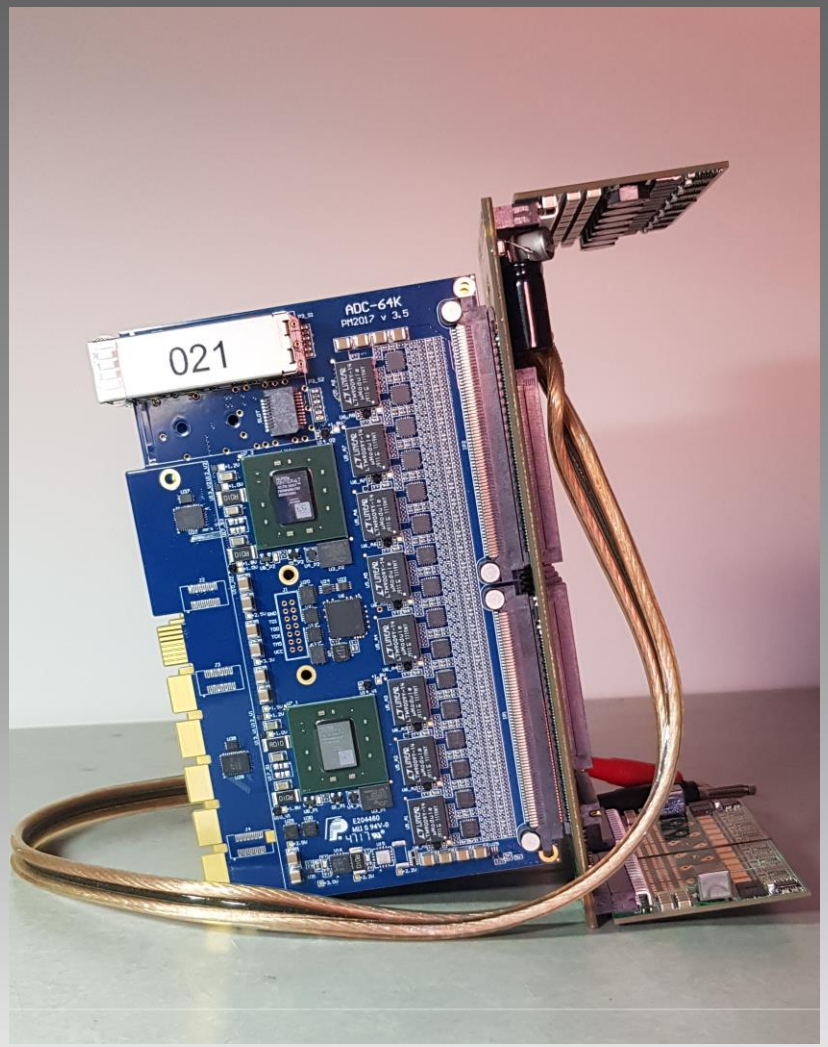




Power Supply







Thank You !