Evaluation of the Kintex7 for the PANDA LMD

PANDA CM 20/1

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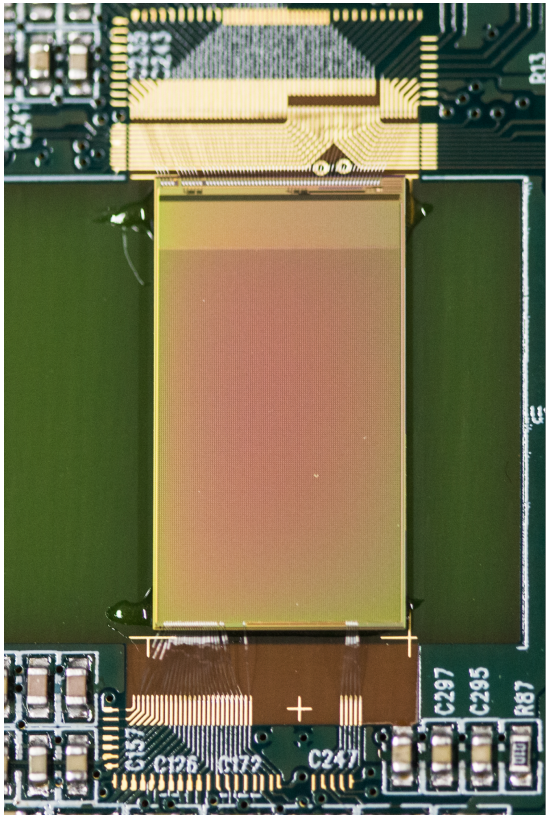
Requirements for FEE

- MuPix read out via 4 LVDS links
- Self triggered with 0 suppression
- External reference clock defines data rate
- Data is 8b/10b encoded

⇒ Asynchronous data stream

⇒ Data Recovery on FPGA necessary

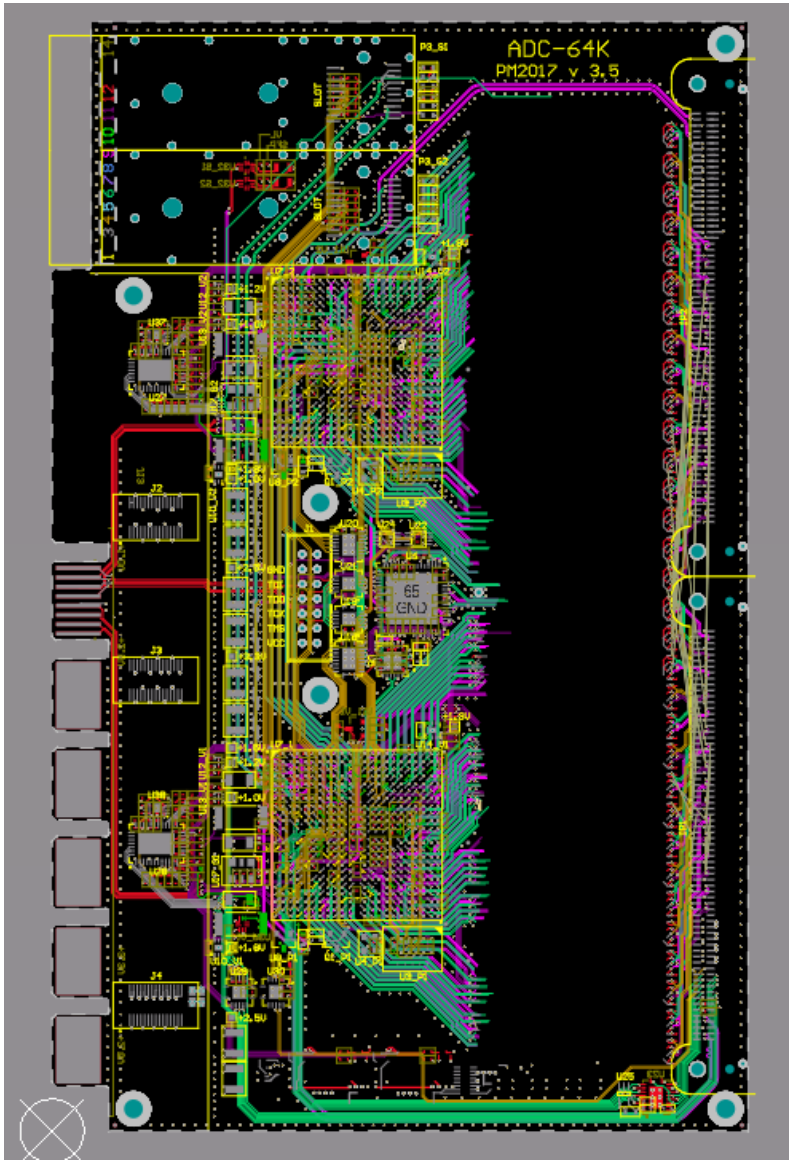
MuPix8 prototype



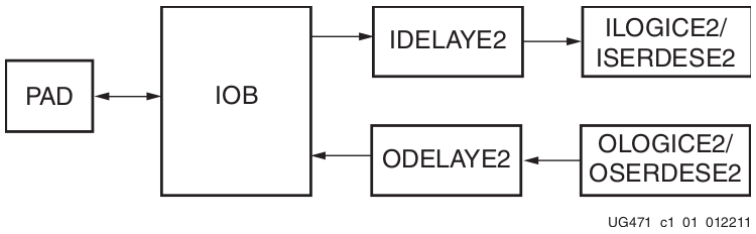
Front-End Board

- Readout Board from Pawel Marciniewski
- Based on EMC digitizer
- Two Xilinx Kintex7 FPGAs (XC7K160T)
- 64 LVDS links per FPGA

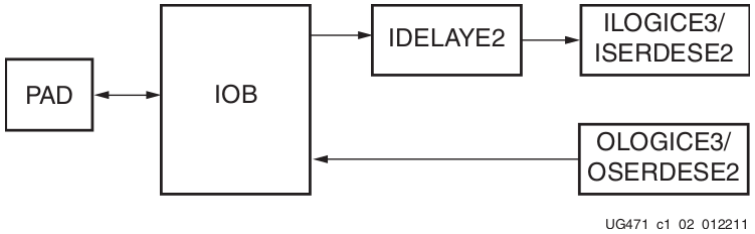
⇒ Up to 16 MuPix chips per board



Kintex7 I/O Pins



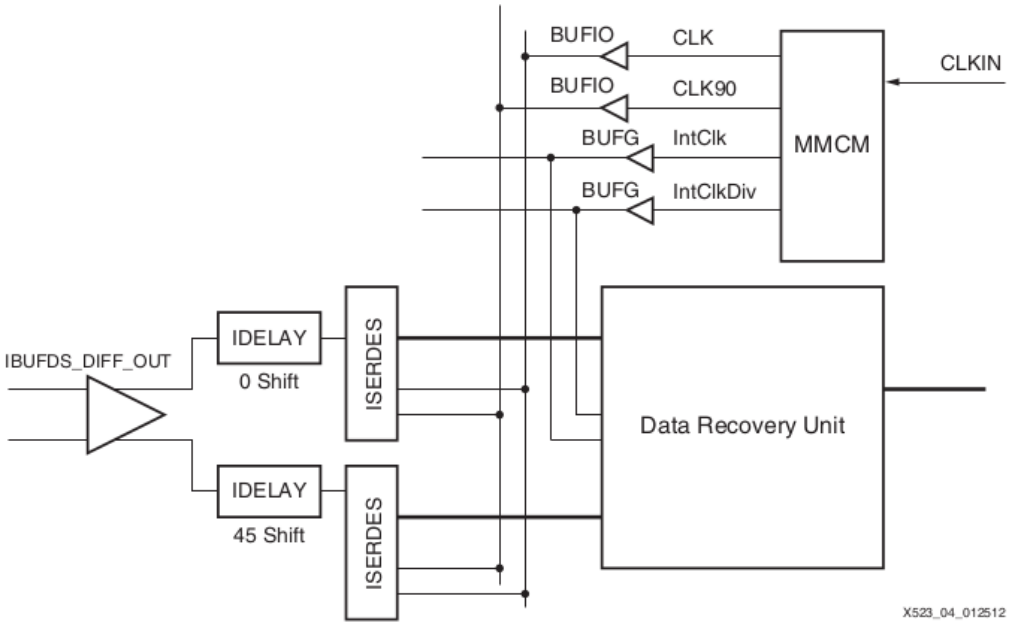
HP Bank I/O tile



HR Bank I/O tile

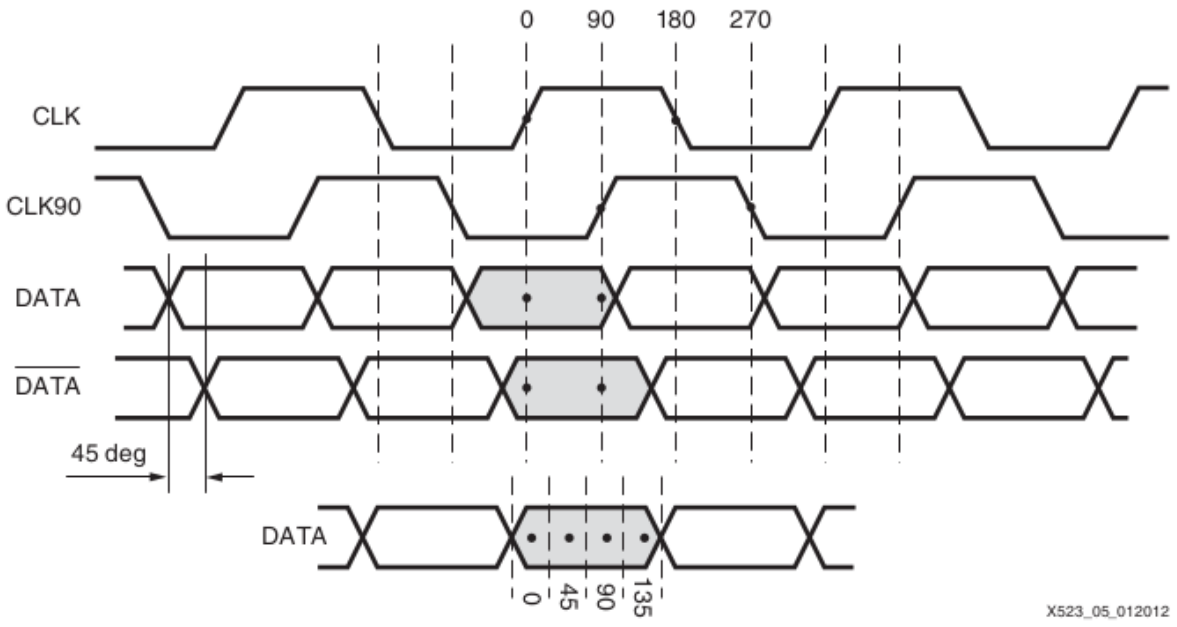
- Each pin of Xilinx 7 series FPGAs has SERDES module for deserialization
- How to determine when to sample incoming data?

Solution 4x Oversampling



- Create two sample clocks with PLL (200 MHz, 90° phase shift)
- Mirror incomming data and phase shift negative signal by 45 degree
- Sample both streams at 0, 90, 180 and 270 degree

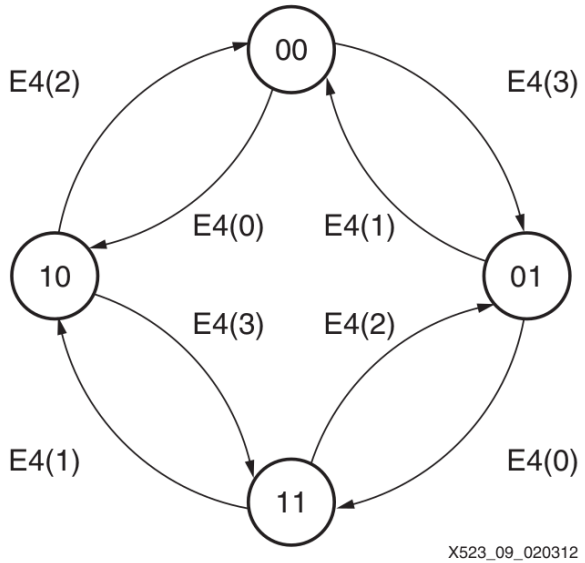
Solution 4x Oversampling



- 8 Sample points for 2 consecutive bits
- Data Recovery Unit (DRU) from Xilinx (XAPP523)

Data Recovery Unit

- Runs at 100 MHz
- State machine compares sample points
- Select two samples (two bits) depending on state:
  - 00: use S_0 and S_4
  - 01: use S_1 and S_5
  - 10: use S_2 and S_6
  - 11: use S_3 and S_7
- Collect 10bit to form output word (on every 2nd/3rd clock cycle)



$$E4(0) = \overline{\left(\overline{S_0} \veebar S_1\right)} \vee \overline{\left(\overline{S_4} \veebar S_5\right)}$$

$$E4(1) = \overline{\left(\overline{S_2} \veebar S_1\right)} \vee \overline{\left(\overline{S_6} \veebar S_5\right)}$$

$$E4(2) = \overline{\left(\overline{S_2} \veebar S_3\right)} \vee \overline{\left(\overline{S_6} \veebar S_7\right)}$$

$$E4(3) = \overline{\left(\overline{S_4} \veebar S_3\right)} \vee \overline{\left(\overline{S_0} \veebar S_7'\right)}$$

Futher data processing

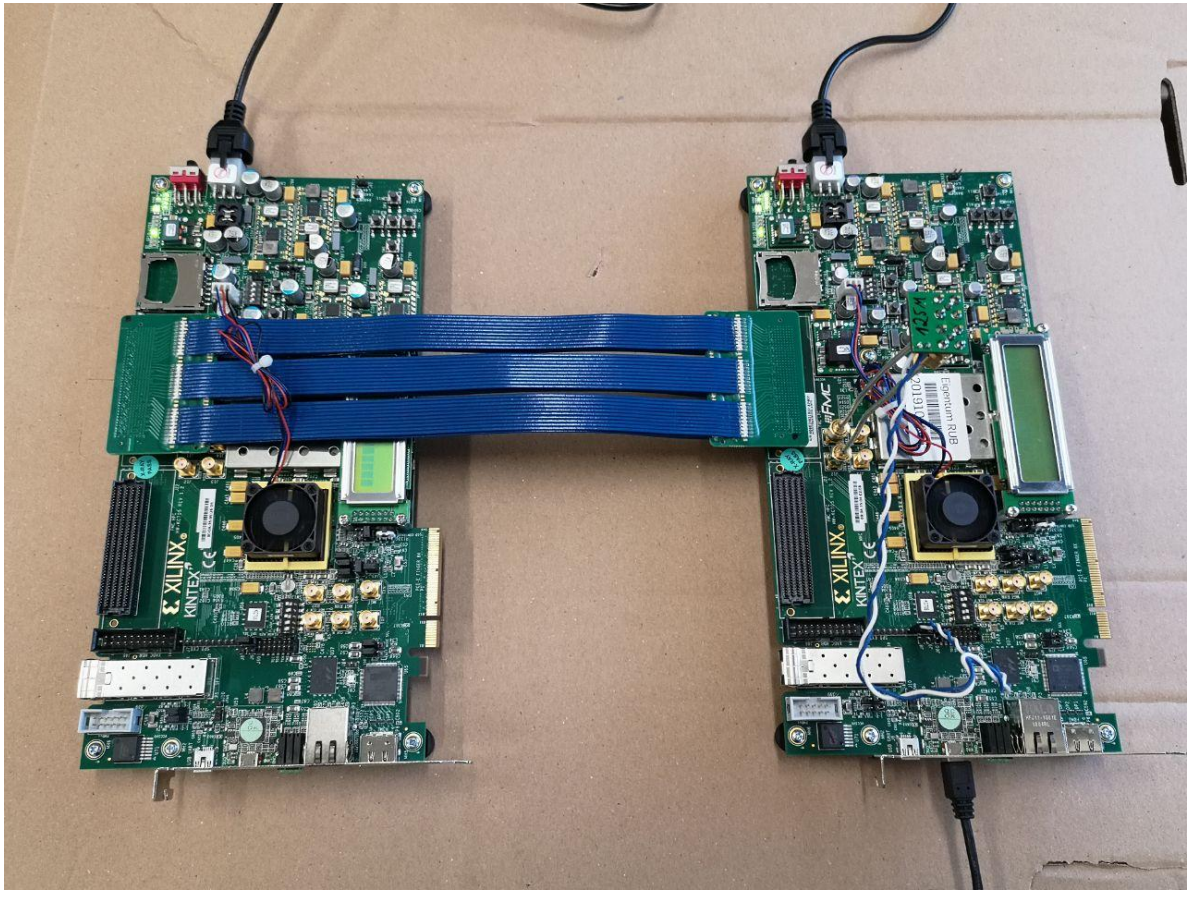
- Start of sampling and first incoming bit have unknown phase shift

$\Rightarrow$ 10bits from DRU are shifted by up to 9bits

$\Rightarrow$ Frame alignment needed

- Buffer two consecutive words (20bit) and search for unique sequence of bits from K28.5 komma word
- Remember position to output aligned 10bit frames
- 8b10b decoding (Xilinx XAPP1112)
- Gray and hit decoding
- Storing hits in async Fifo

First Tests in Lab



Tests data recovery with up to 1.25 Gbit s^{-1}
So far no tests with real MuPix (Adapter board is delayed)

Utilization

Needed resources per receiver channel:

Unit	# Slices
DRU	10
Frame align	10
8b10b decoding	2
$\sum$	22

Beam time

Next beamtime at COSY: 23rd - 28th of March