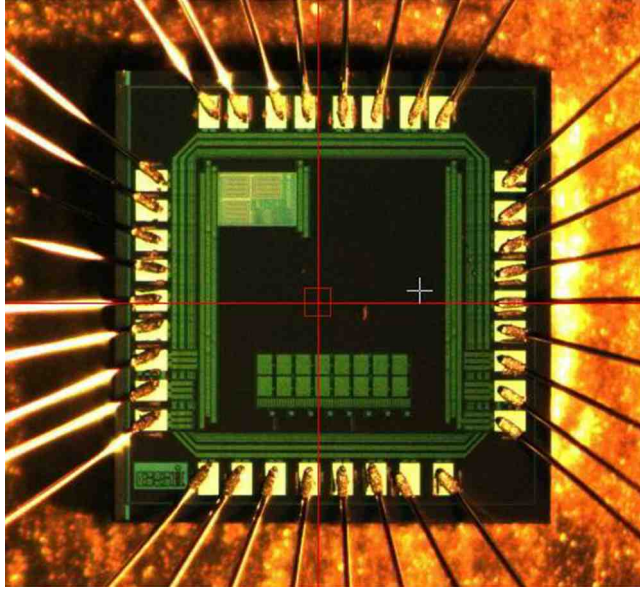
Recent developments of the slow-control of the barrel part of the PANDA EMC front-end bus system



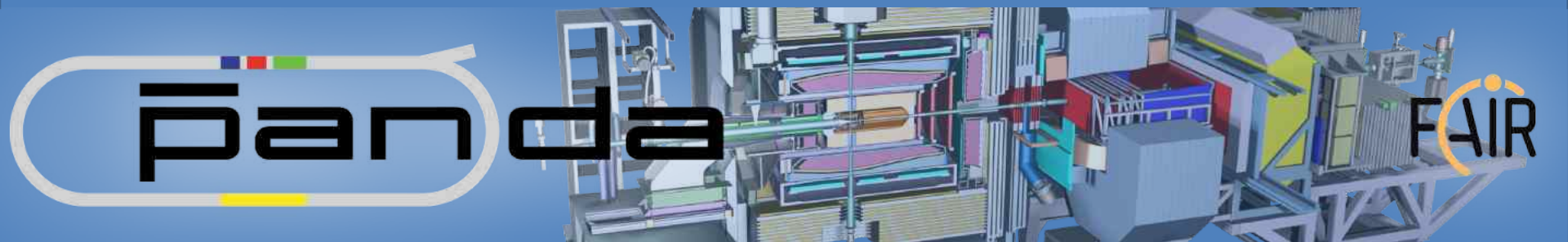
Federal Ministry of Education and Research

JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

GSI

Christopher Hahn* for the PANDA collaboration
*2nd Physics Institute, University Giessen, Germany

HIC for FAIR
Helmholtz International Center



Outline

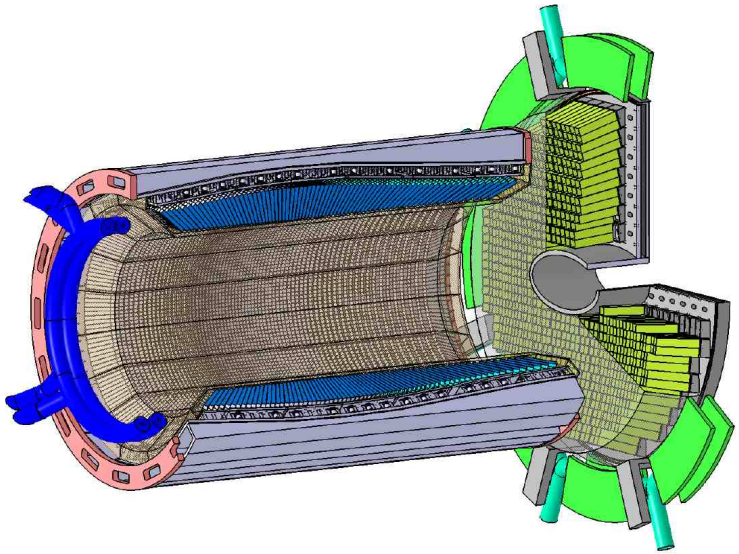
- **Overview**
- **High-voltage measurements**
- **Impact of different SerialAdapterASIC DAC accurancy on resulting high-voltage**
    - V100 (old)
    - V110 (new)
- **Conclusion and outlook**

Overview

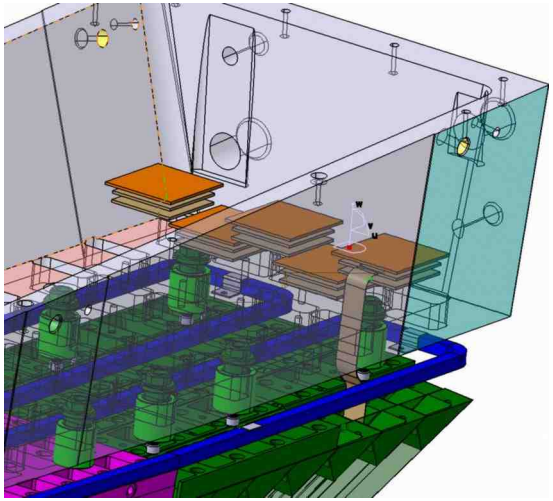
- 11360 PbWO crystals in PANDA Barrel EMC (in 16 slices) [4]
- 22720 large-area **a**valanche **p**hoto **d**iodes (APDs)

  → each APD needs individual adjustable high voltage

  → voltage adjustment within the slice

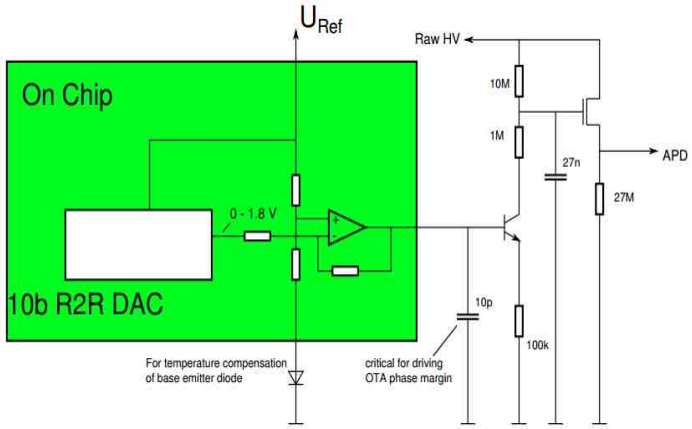


- **Present design: 3 Layers**
- HV distribution & regulation
- Connector board for custom signal cables
- Board for FlexPCBs / ASICS
- Connectors to FEs
- 8x2 Diff. Line drivers
- APFEL I/F buffers
- Temp/Humidity sensors

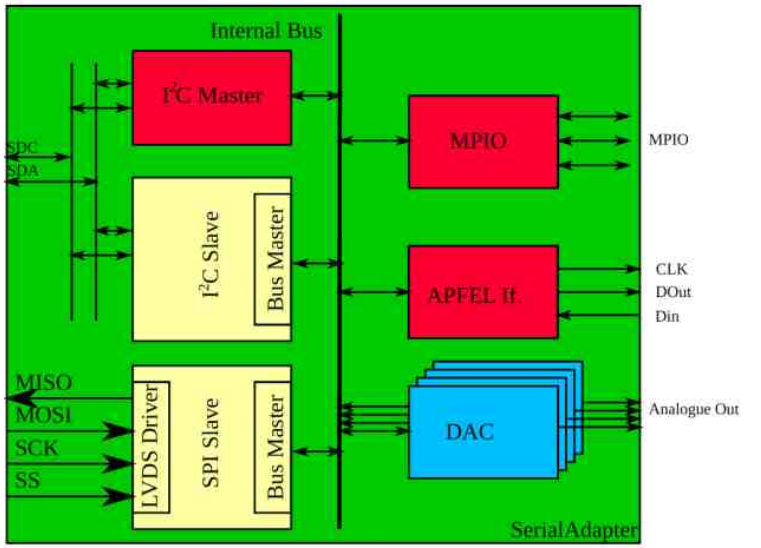


High voltage distribution

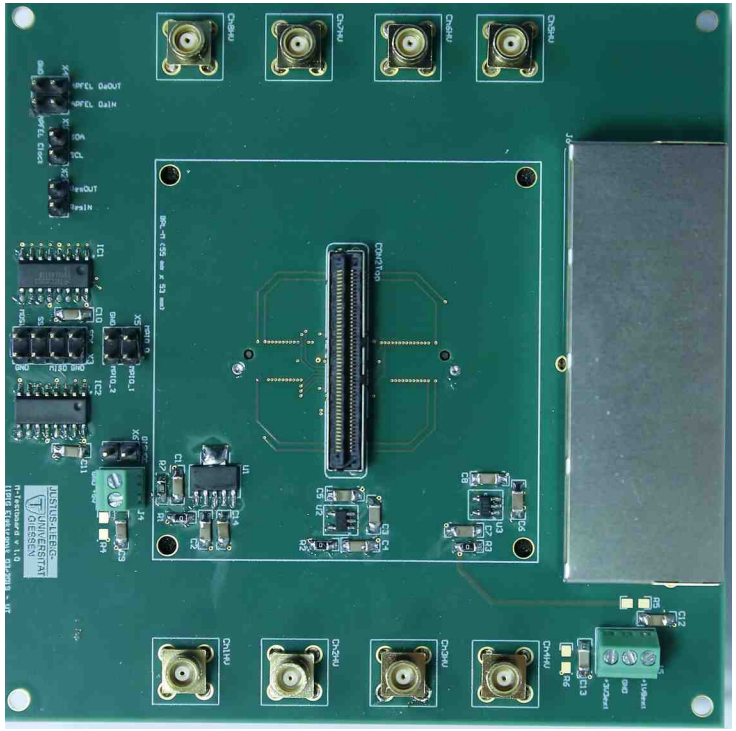
- Device to independently adjust bias voltage of 8 APDs with one HV-source channel
- 50V from HV input downwards in <0.1V steps
- All channels fed from the same HV source
- Online measurement of APD voltage and current

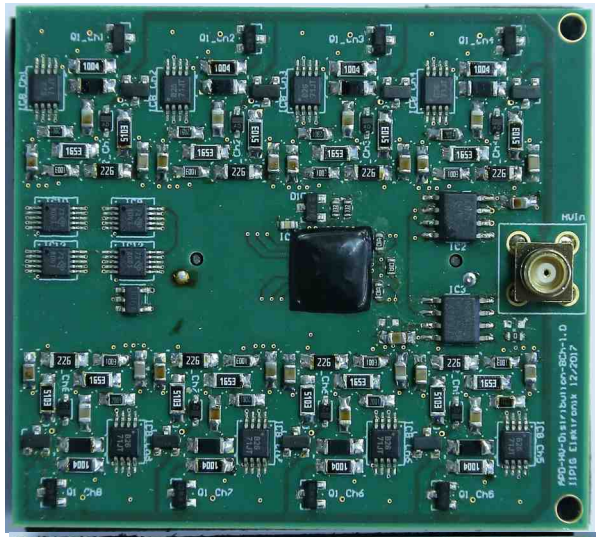


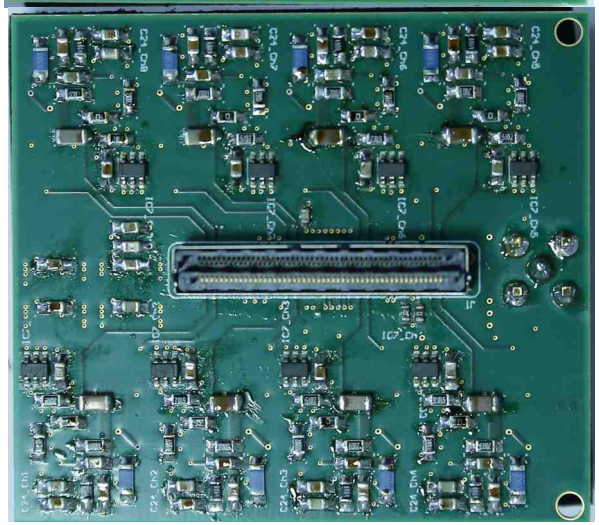
- **SerialAdapterASIC**: integrated slow control ASIC with common interfaces (I2C, SPI and APFEL interface)
- Daisy chaining of Backend-Interface for 5 (10) backplane PCBs → Saves 4/5 of slow control cables (36 vs. 180**)**
- Use DACs for HV adjustment

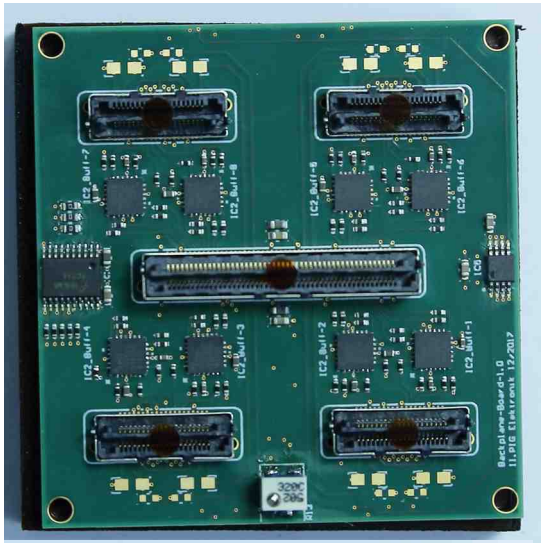


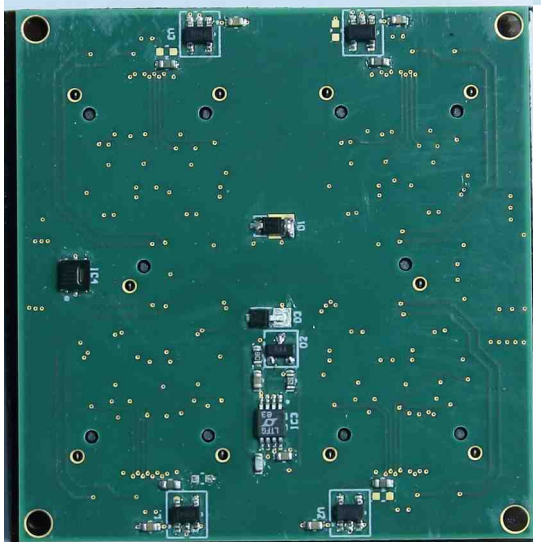
Overview





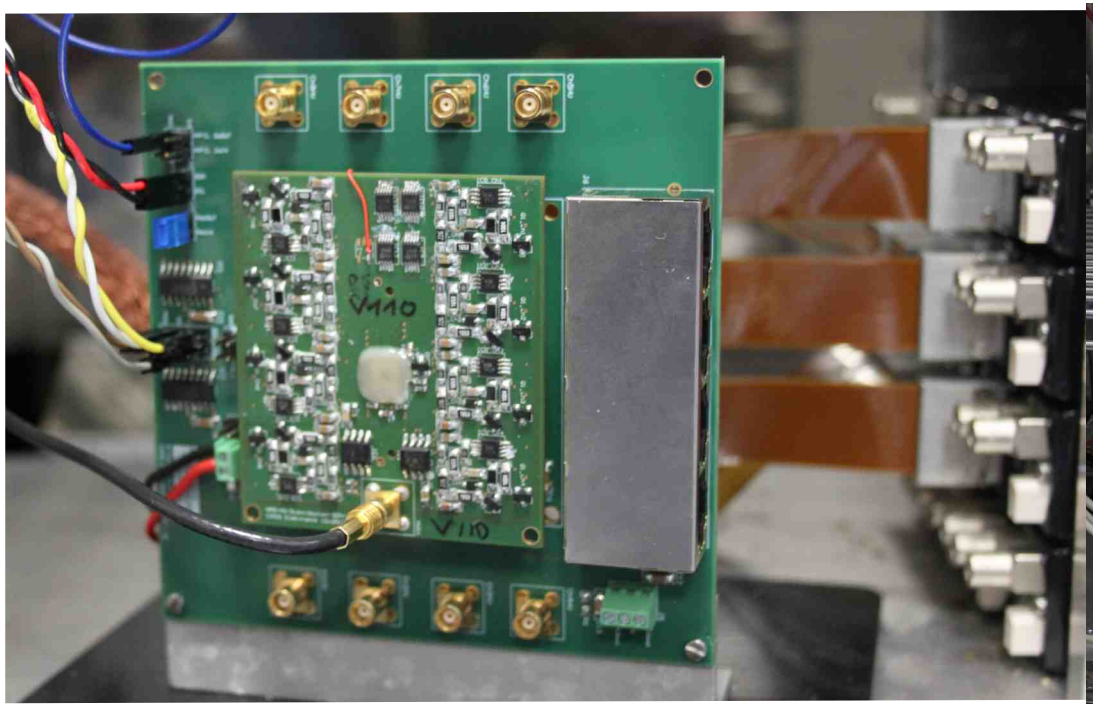


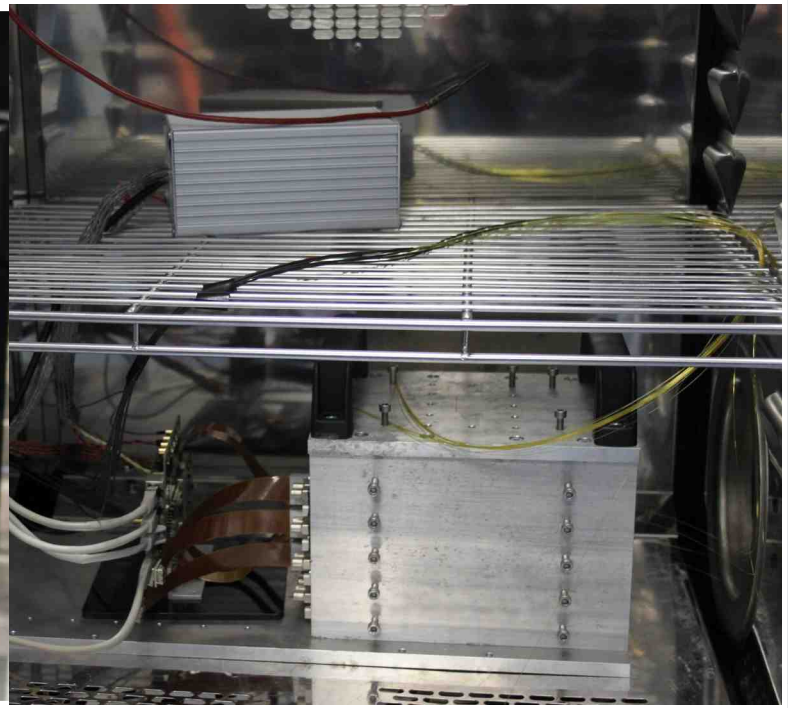




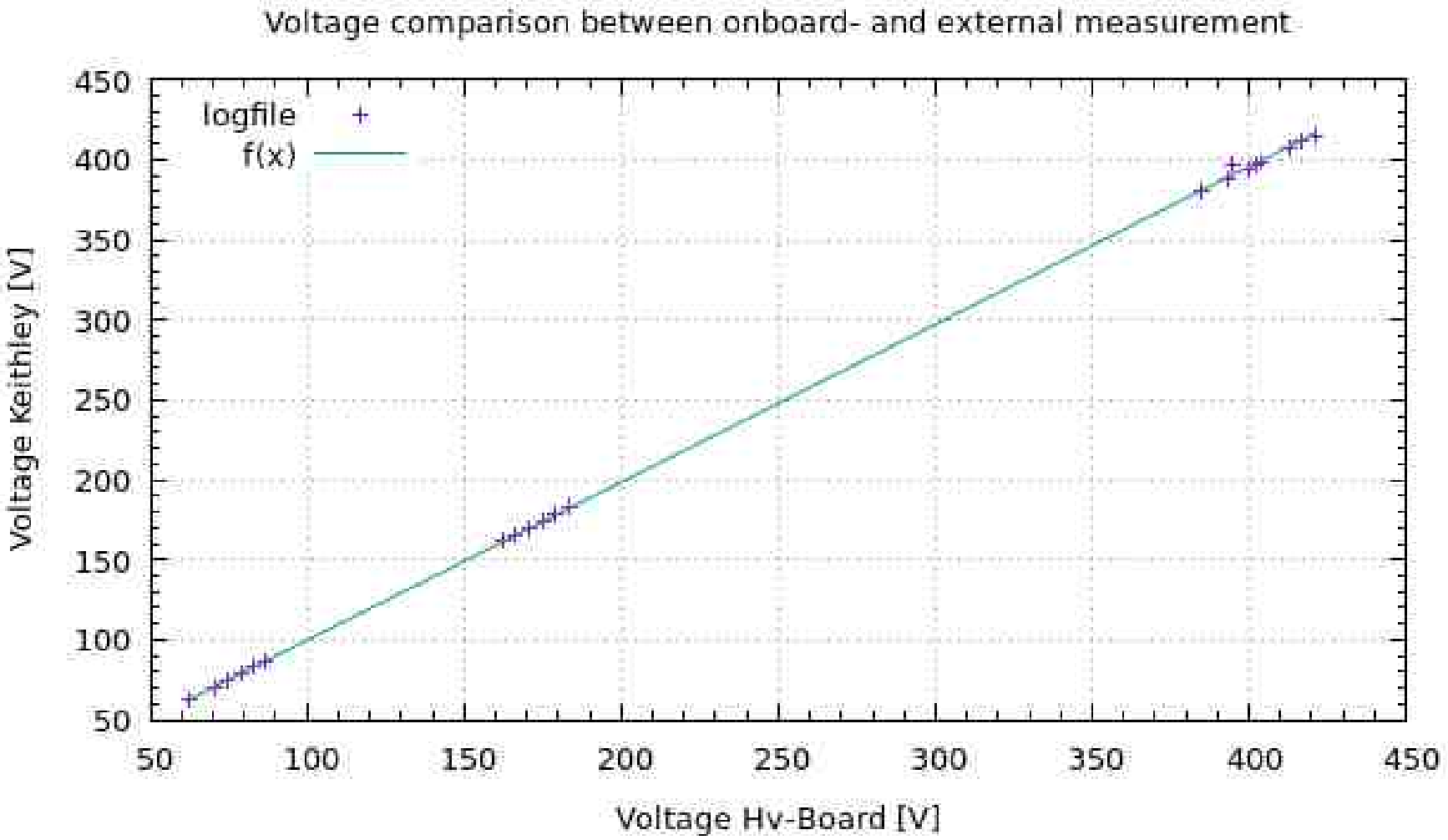
Overview

- **Full triple sandwich setup as test system**
- **System tests can be undertaken under room temperature and at -25°C**
- **Verification of the onboard voltage measurement was undertaken**
- **Impact of different DAC versions on resulting HV was studied**

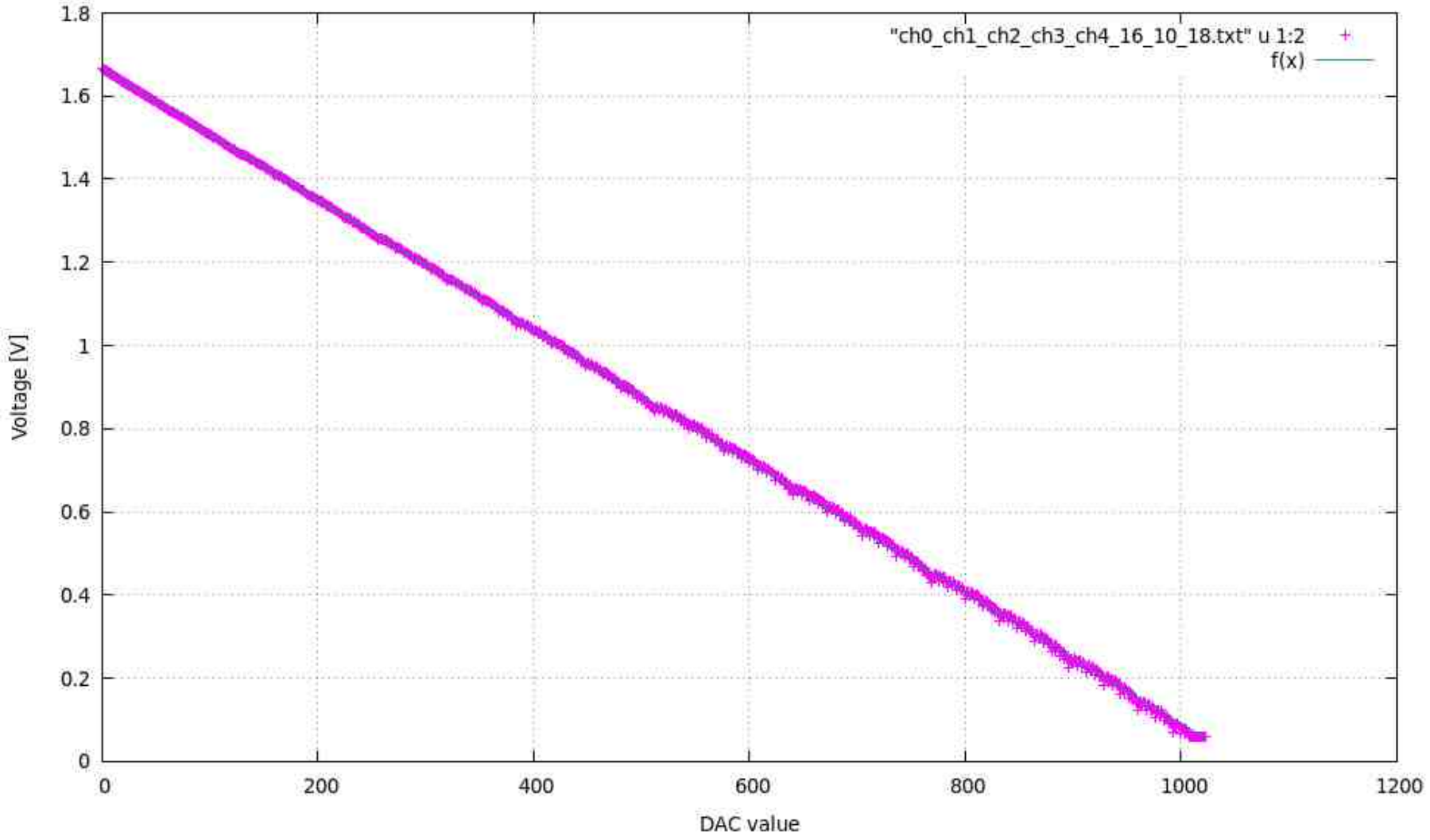




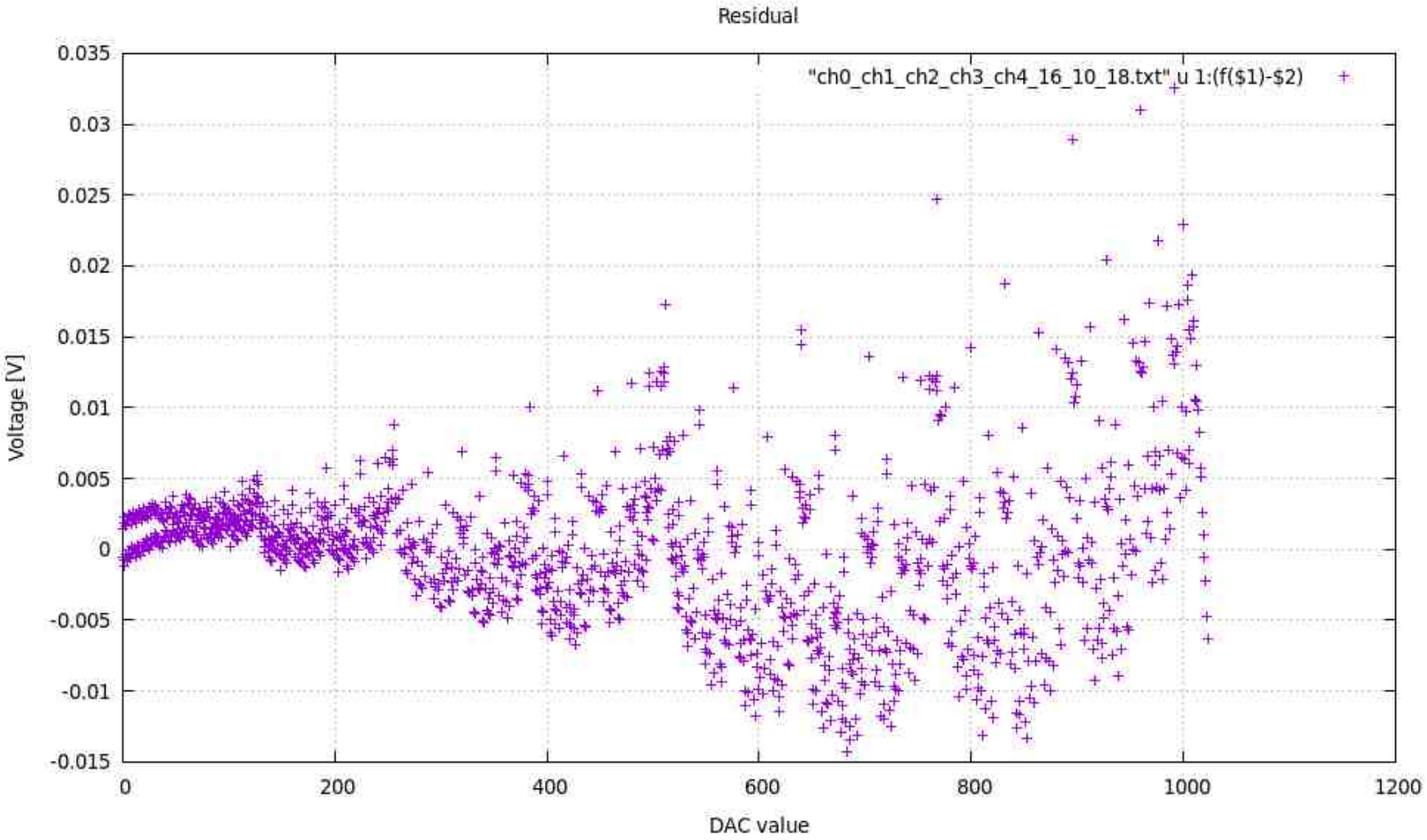
Comparison between onboard measured high-voltage and external measured high-voltage



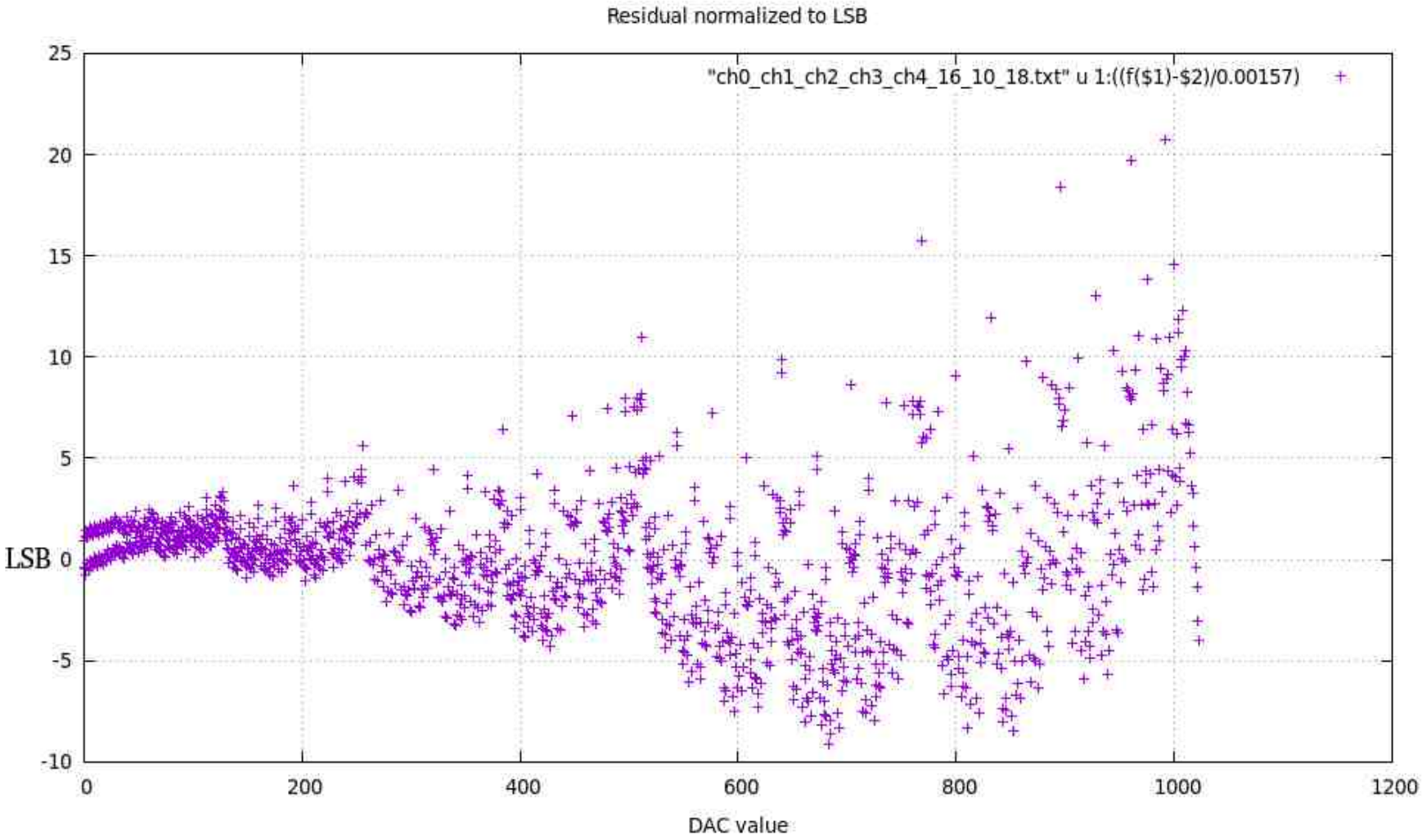
SerialAdapterASIC - DAC Measurements - V100



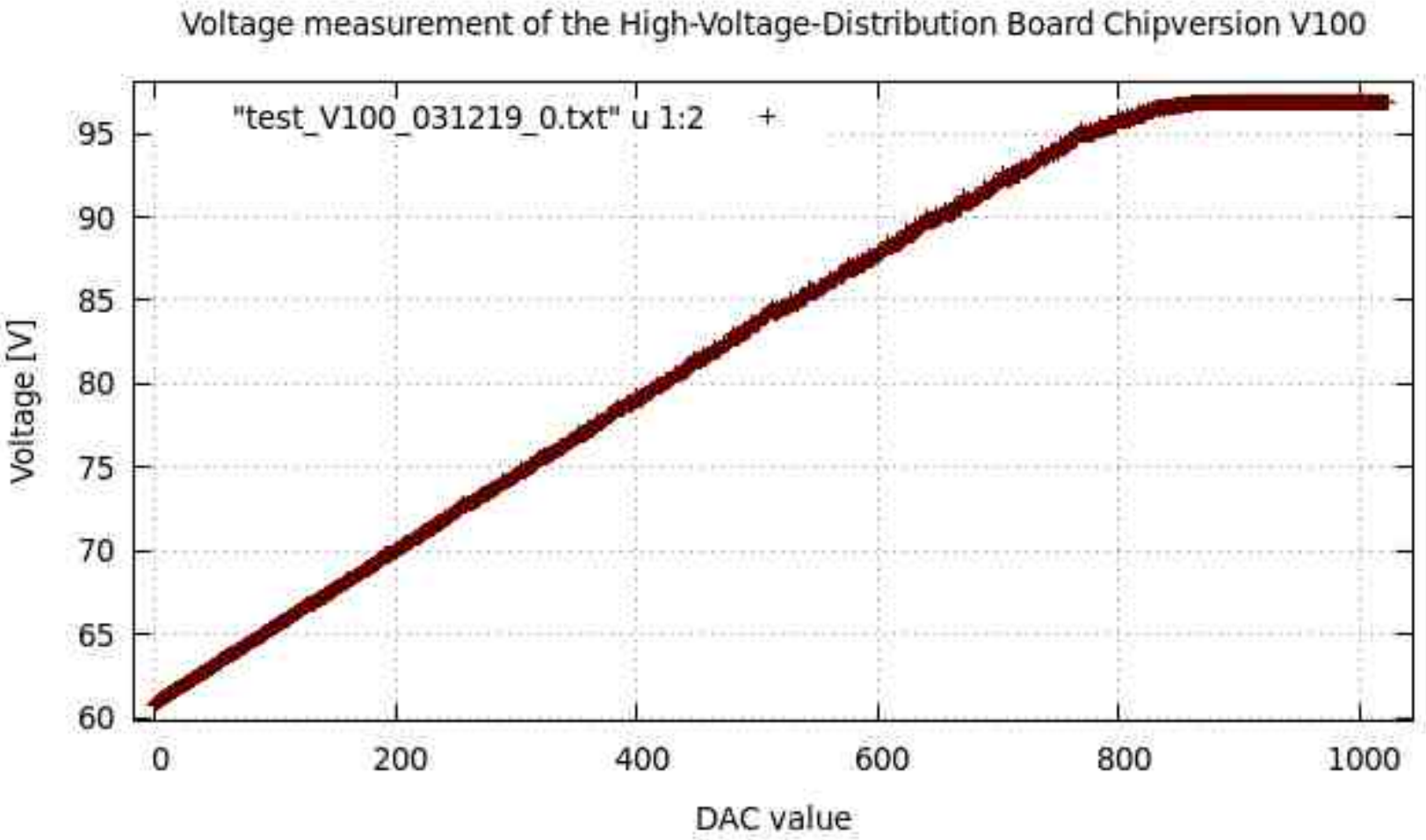
SerialAdapterASIC - DAC Measurements - V100



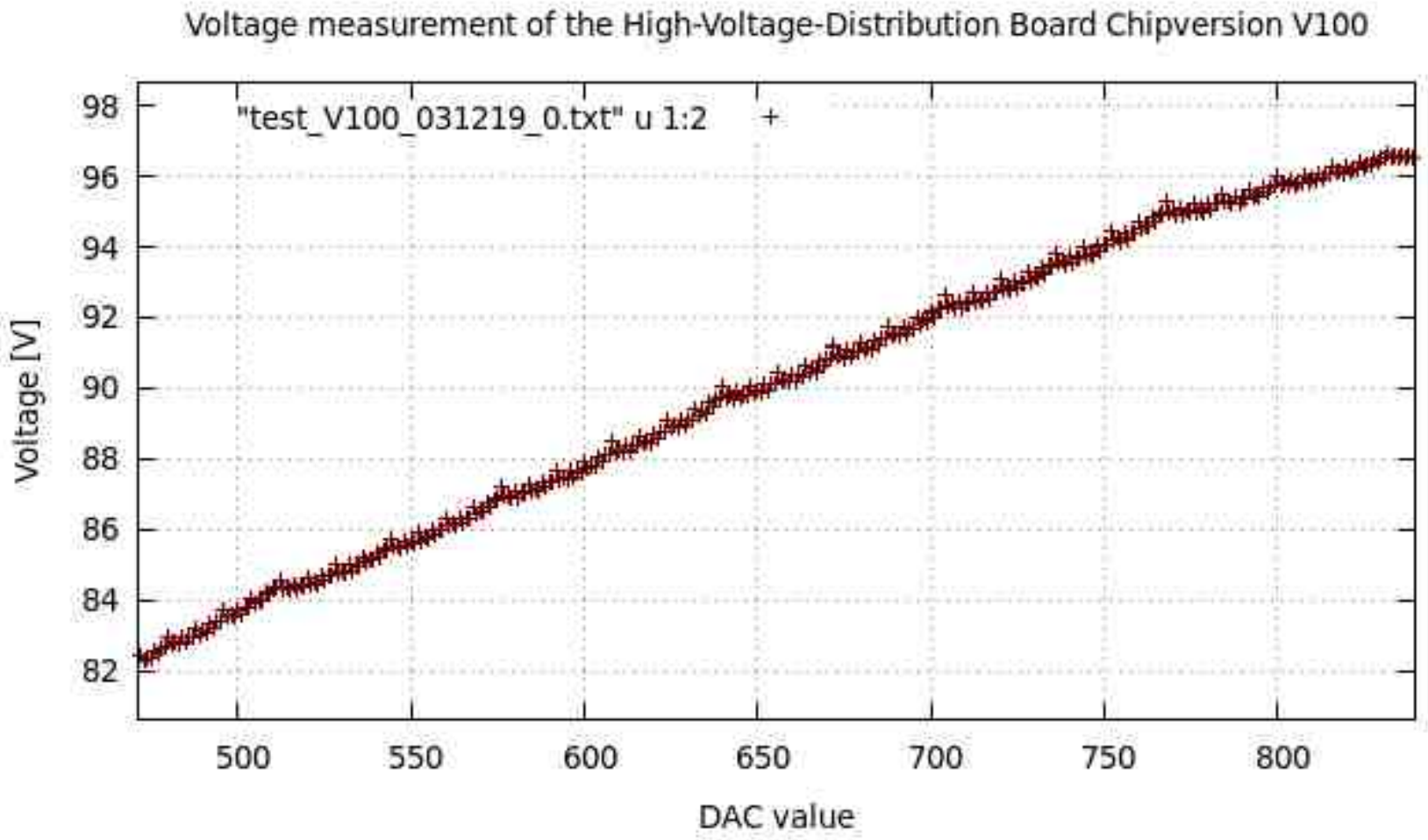
SerialAdapterASIC - DAC Measurements - V100



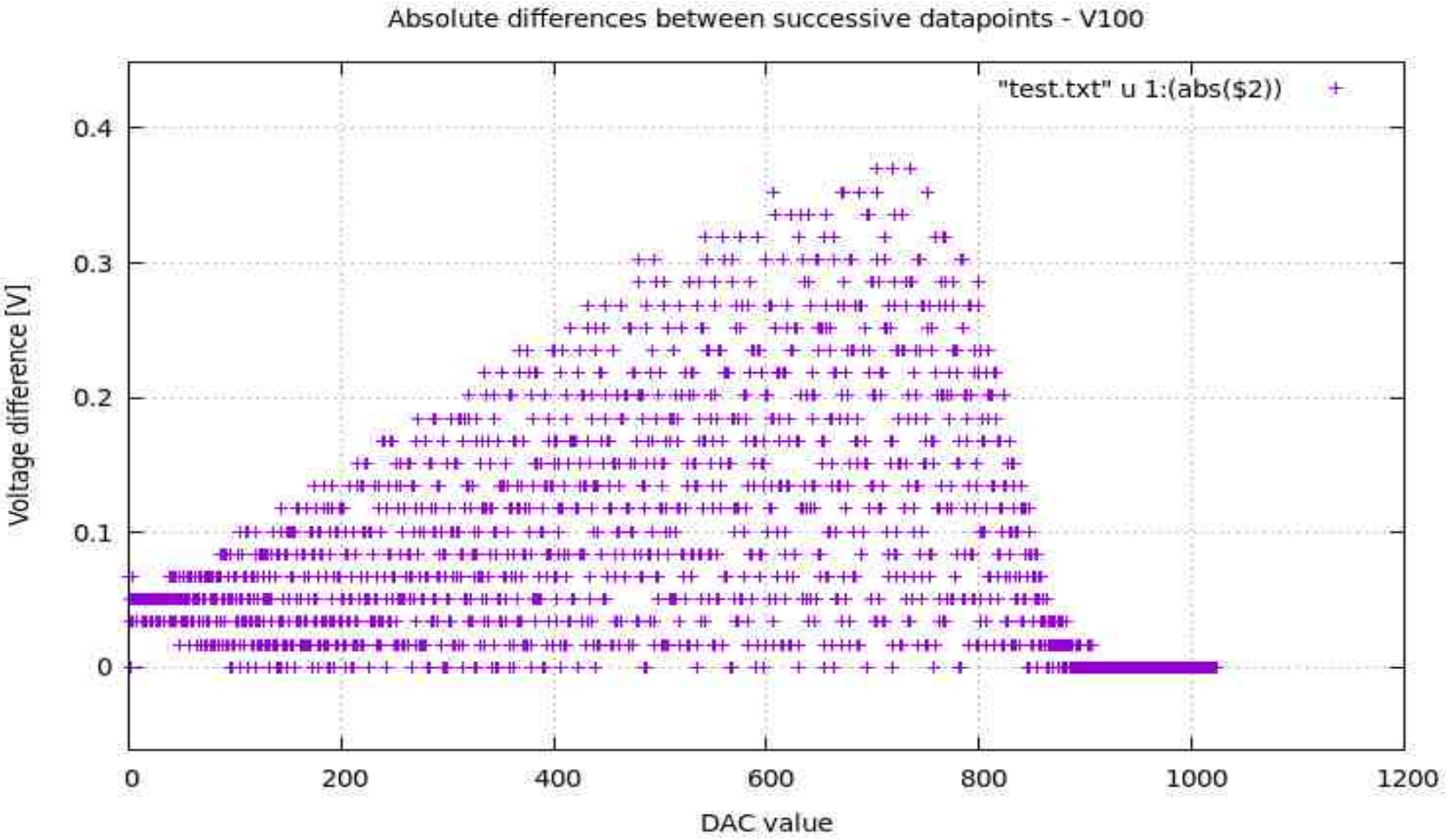
Impact on HV – SerialAdapterASIC V110



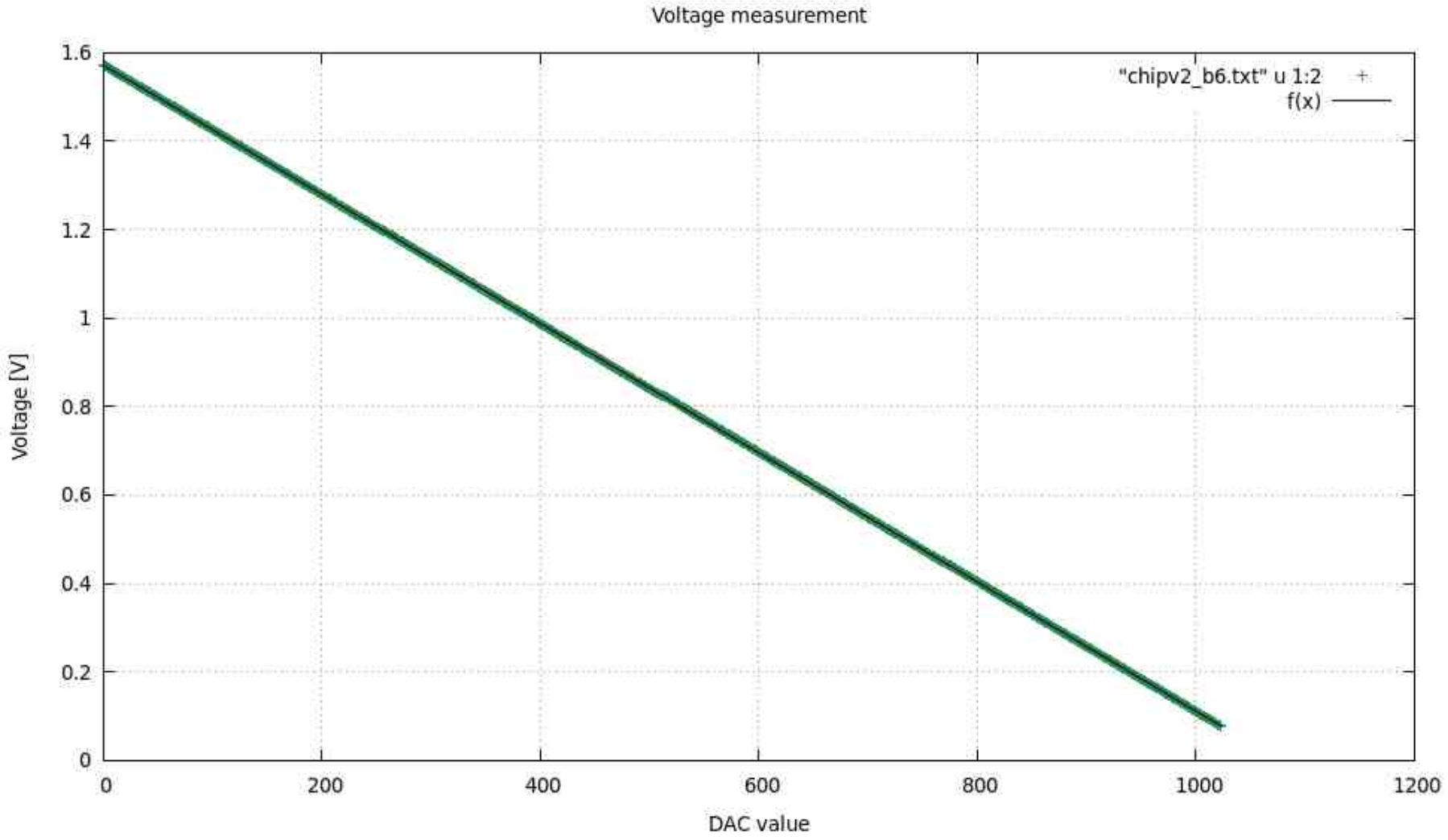
Impact on HV – SerialAdapterASIC V110 (zoomed)



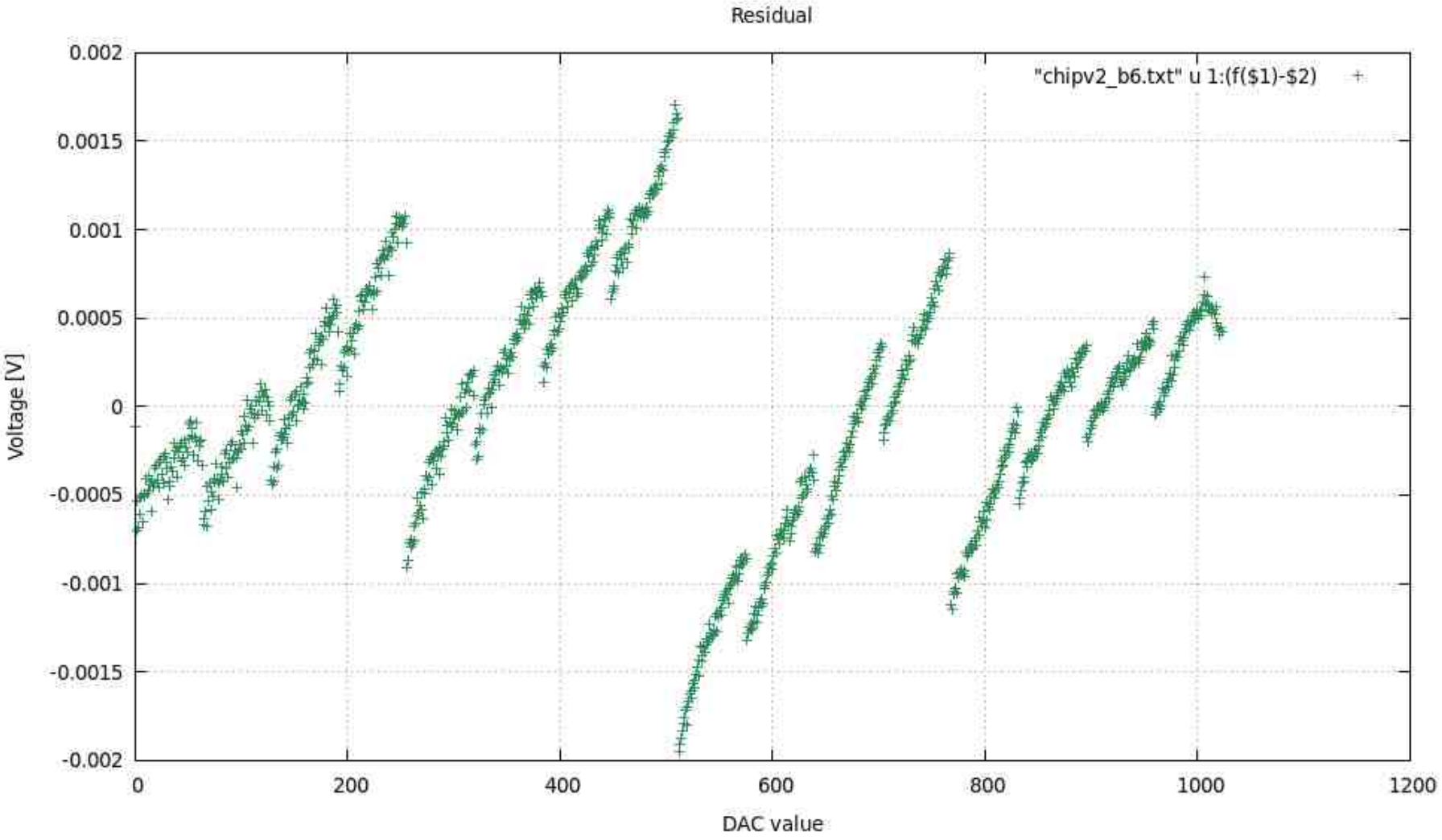
Impact on HV – SerialAdapterASIC V110 (as differences)



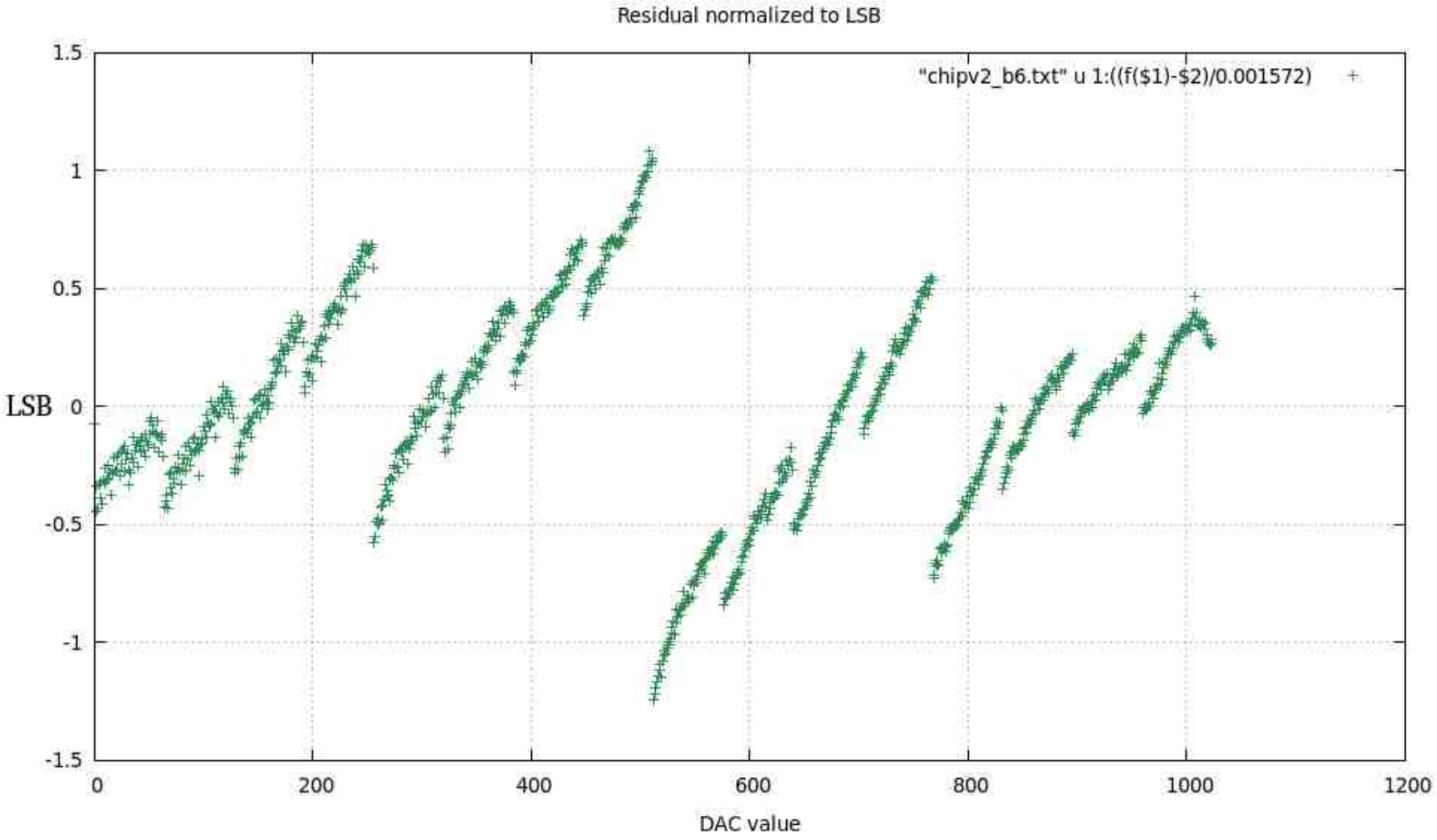
SerialAdapterASIC - DAC Measurements – V110



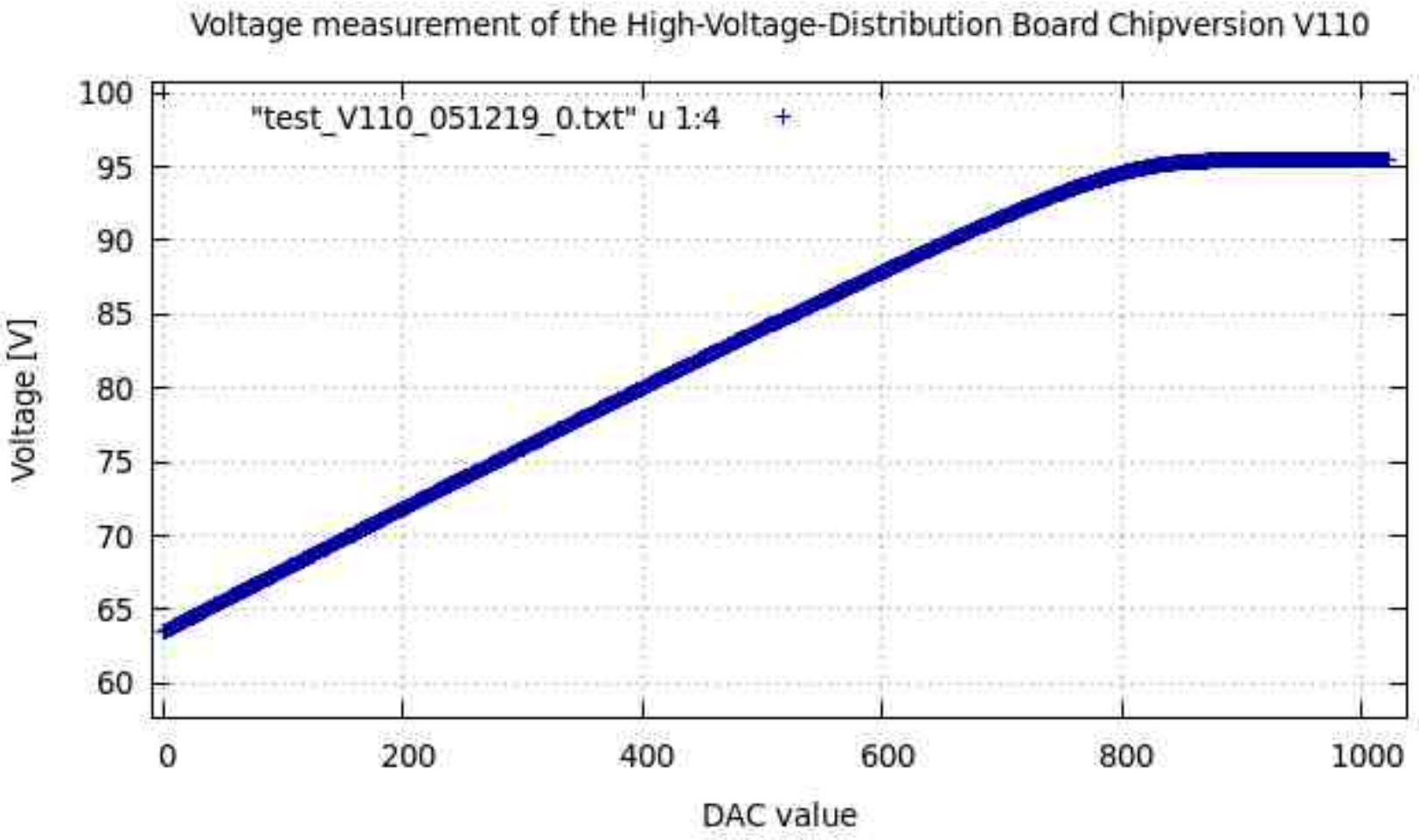
SerialAdapterASIC - DAC Measurements – V110



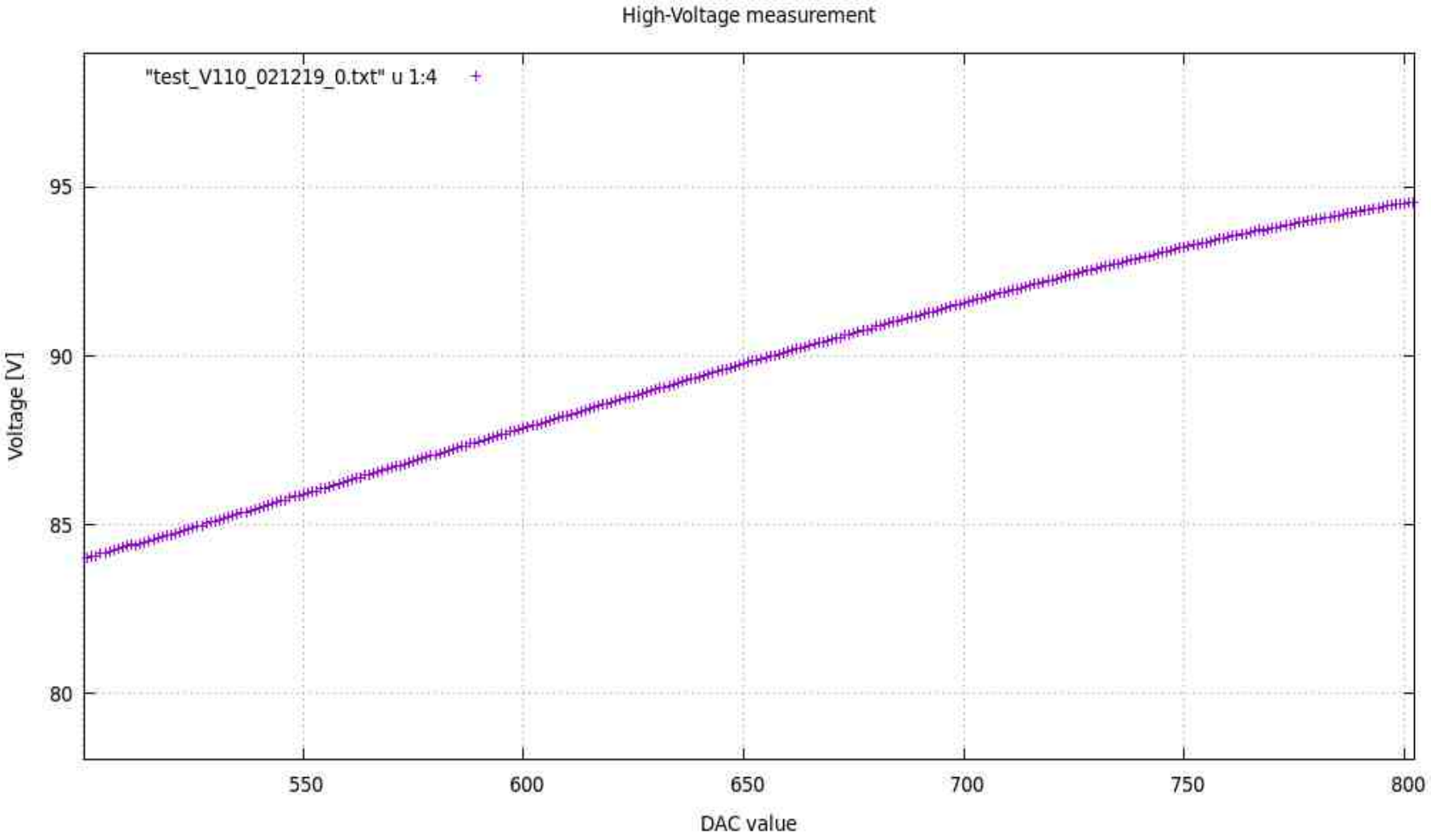
SerialAdapterASIC - DAC Measurements – V110



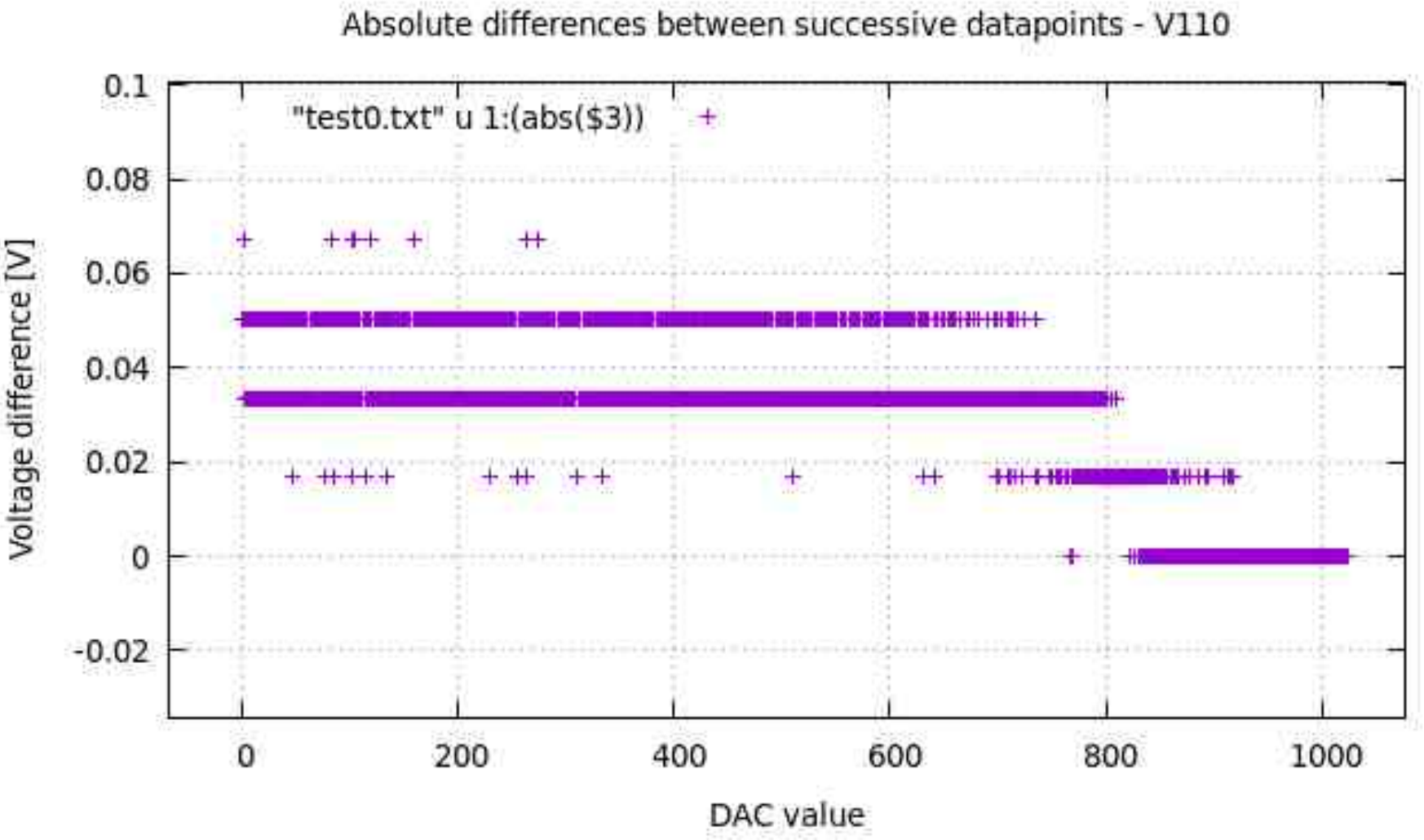
Impact on HV – SerialAdapterASIC - V110



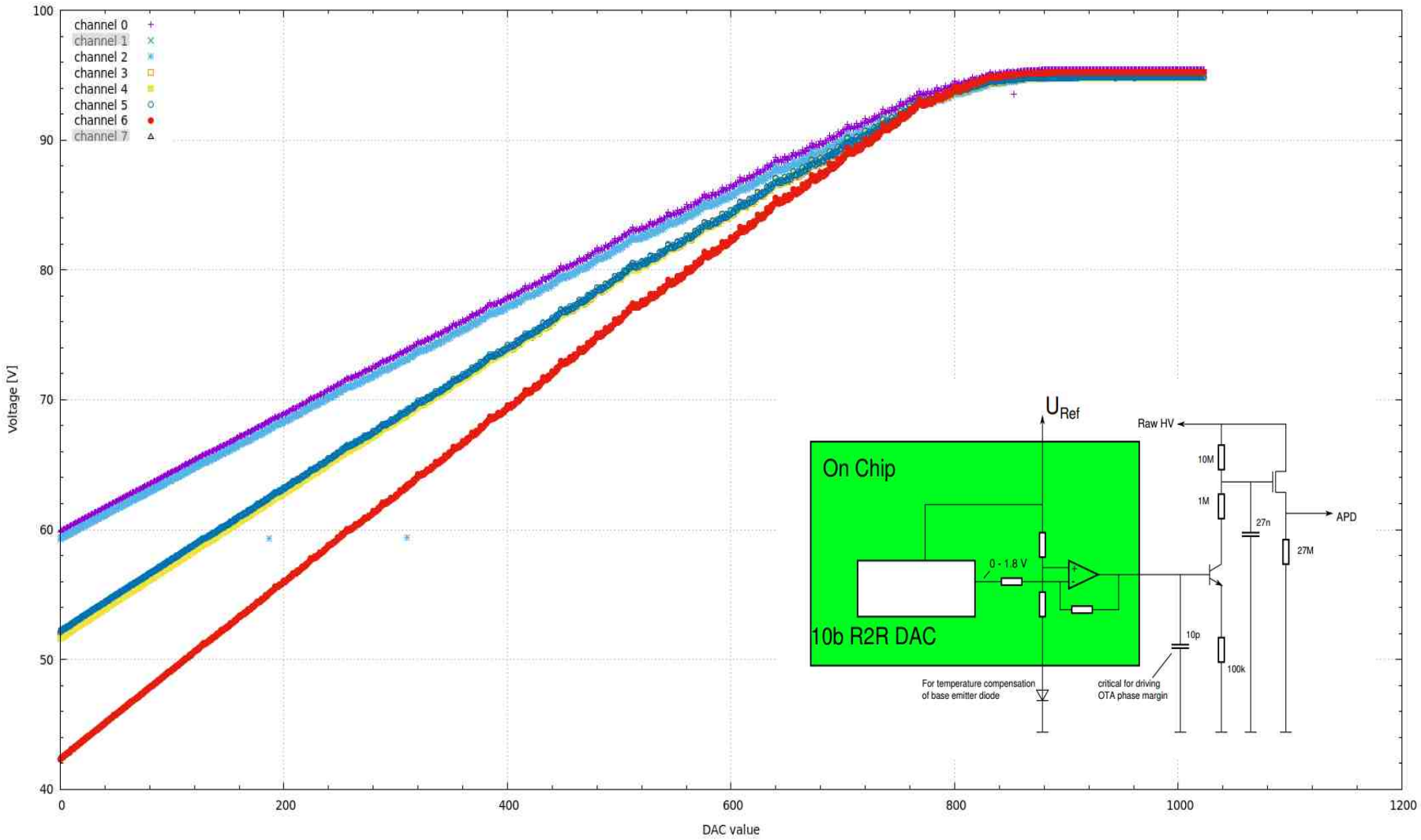
Impact on HV – SerialAdapterASIC - V110 (zoomed)



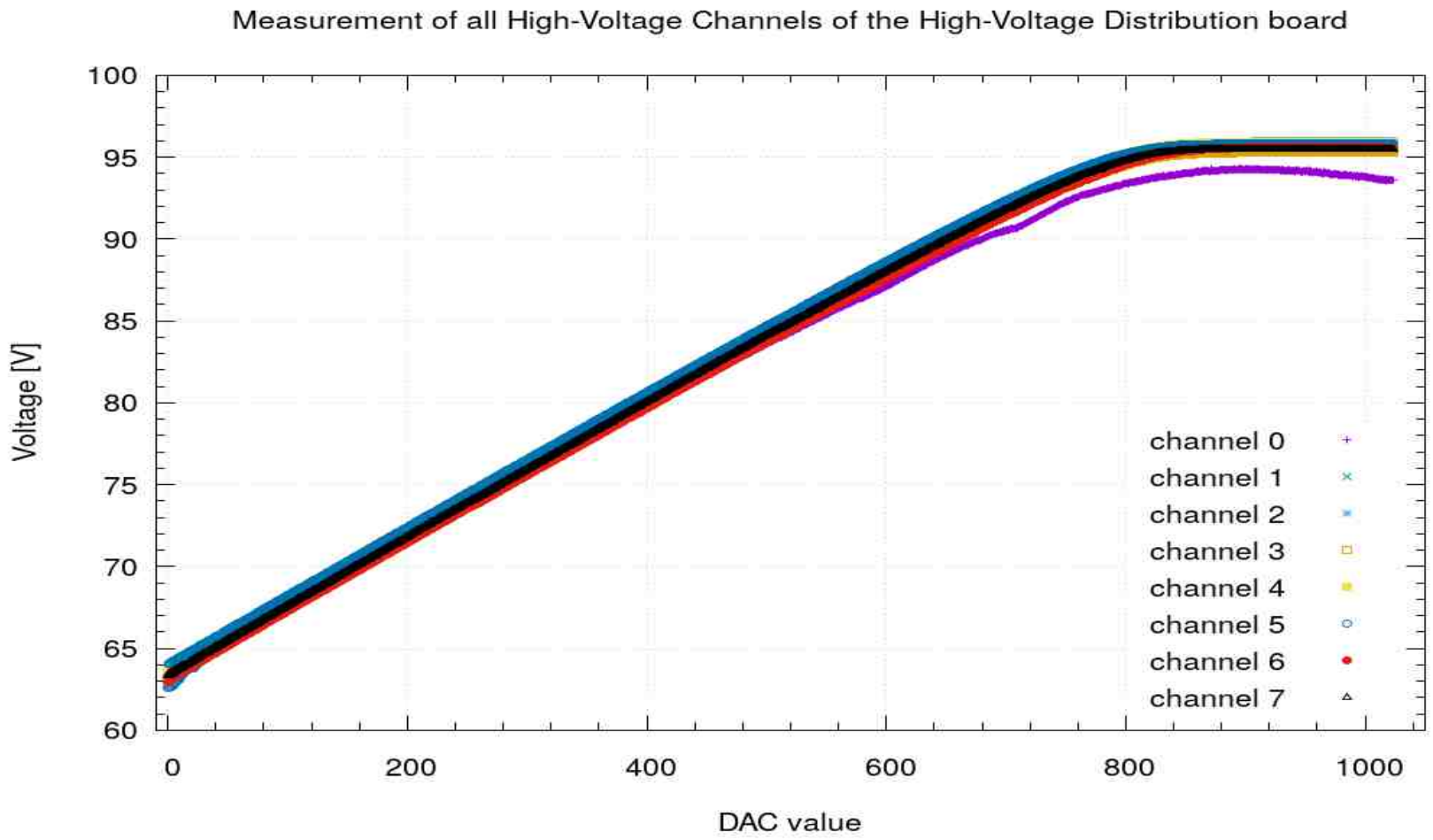
Impact on HV - SerialAdapterASIC - V110 (as differences)



Impact of different regulating resistors
SerialAdapterASIC - V110

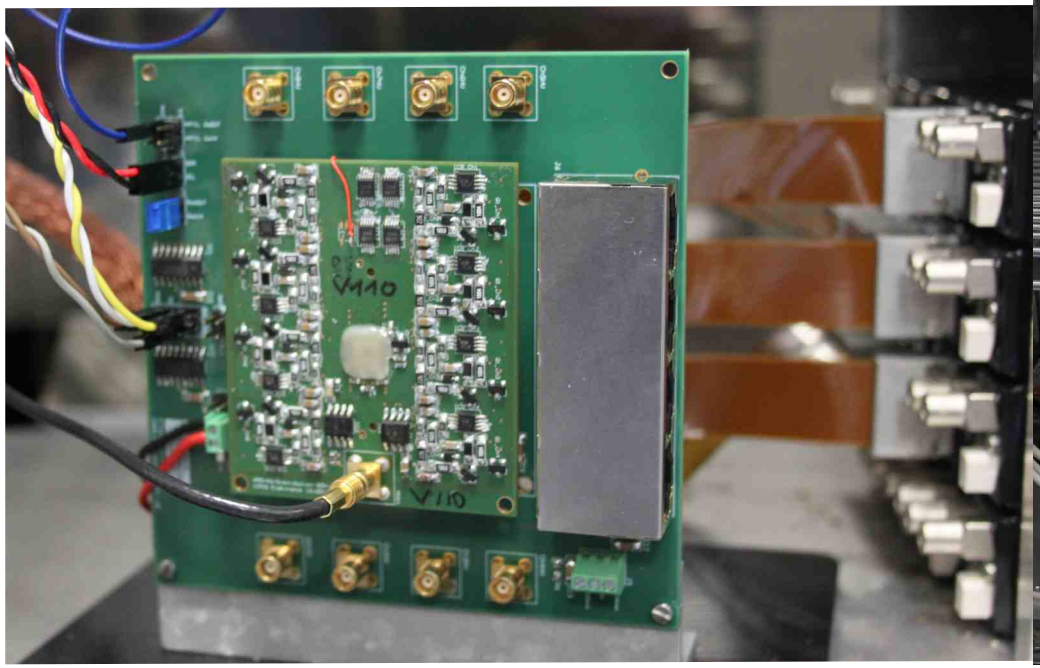


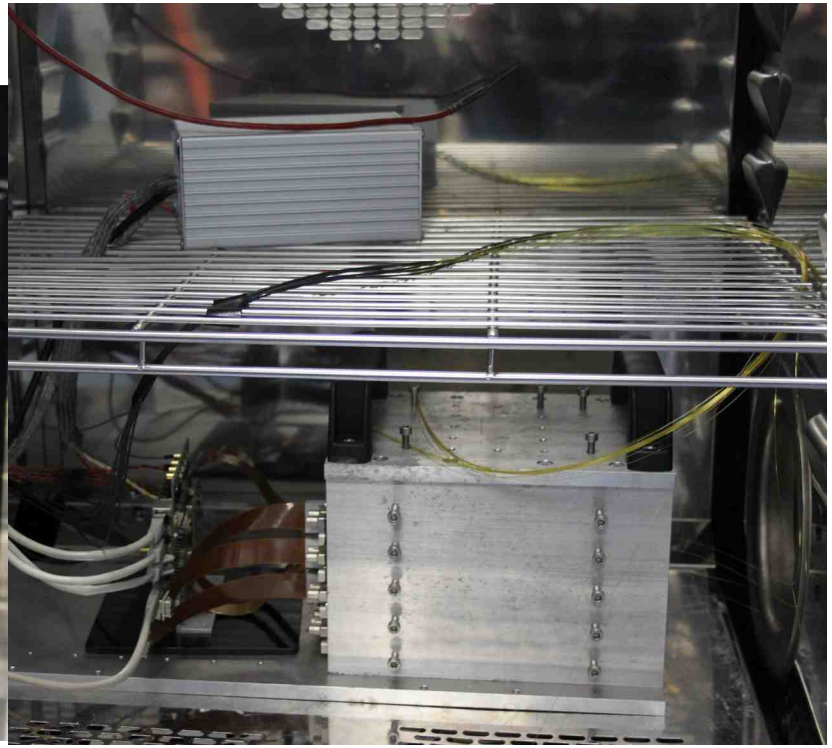
All HV-Channels - SerialAdapterASIC - V100



Pulser tests

- **Full tripple sandwich setup connected to 4 PbWO crystals as test system**
- **System tests undertaken under room temperature and at -25°C**
- **Pulser tests look promising**





Pulser tests

Conclusion and outlook

- **Great Improvement between DAC V100 and V110**
- **Minor bugs on the PCBs were fixed**
- **High-voltage Regulation width can be tweaked a little bit**
- **First tests with a full readout chain look promising**
- **Next PCB iteration will be the final prototype**

  → if there are no problems in production and tests

  this PCB will be serialized, calibrated in the current setup and

  used in the slice